Energy Storage System of the Converted Discharge Energy under VLF Testing Conditions

Master Thesis

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Declaration in Lieu of Oath

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Kurzfassung

Hochspannungskabel spielen in Stromverteilungsnetzen eine bedeutende Rolle. Isolationsfehler in Kabeln verursachen negative Auswirkungen auf das Betriebsverhalten. Anhand einer Wechselspannungsprüfung mit einem niederfrequenten Hochspannungsgenerator, erfolgt die Beurteilung der Isolationsqualität. Diese Generatoren erzeugen dafür eine sinusförmige Prüfspannungen von $0.1\mathrm{Hz}$ mit Spannungswerten bis zu $65\mathrm{kV}$. Während der Qualitätsprüfung wird das Kabel wiederholt geladen und entladen. Der Entladevorgang am Kabel erfolgt über einen Entladekreis, in dem die Energie thermisch abgeleitet wird. Um diese Energie elektrisch wieder zu nutzen, soll eine neuartige Erweiterung in Form eines Energiespeichersystems vorgestellt werden.

Diese Arbeit beschreibt den Designprozess eines Energiespeichersystems, das die Zwischenspeicherung der Entladeenergie ermöglicht. Das entwickelte System besteht aus einem bidirektionalen DC/DC-Wandler und einem Aluminium-Elektrolytkondensator. Der Energiespeicher ist auf die maximale Generatorleistung dimensioniert. Die effektive Regelung des Leistungsflusses zwischen Speichersystem und der verfügbaren Entladeenergie, erfolgt durch einen synchronen Buck-Boost Wandler. Zusammen mit einer theoretischen Analyse der zugrundeliegenden Problemstellung und der Anwendung von Wandler Analysemethoden, wurde die Dimensionierung des Wandlers durchgeführt. Darüber hinaus wurde ein Zustandsraummodell erstellt, um das Regelungssystem zu entwerfen. Implementiert ist eine Eingangsstromregelung anhand eines PI-Reglers. Die Bewertung des Systems erfolgt durch eine modellbasierte Hardware-Implementierung in Matlab Simulink und Plecs Blockset. Das System ist in der Lage, Entladeenergien von bis zu $4.3\mathrm{kJ}$ in einer kurzen Ladezeit von $2.5\mathrm{s}$ zwischenzuspeichern. Die maximale Spitzenleistung während der Ladephase beträgt $2.7\mathrm{kW}$. Basierend auf einer C-Code-Implementierung des digitalen Reglers, erfolgt eine hardwarenahe Simulationsstudie. Während des Designprozesses wurden theoretische Berechnungen durchgeführt. Diese zeigen, dass der Entwurf eines Speichermediums einen direkten Einfluss auf die Spitzenströme des Systems haben und auch die zulässigen Gleichspannungsbereiche der elektrischen Komponenten einschränken. Das entwickelte Energiespeichersystem und die Strategie zur Leistungsflussregulierung wurden durch Simulationsstudien untersucht. Die Ergebnisse zeigen eine ordnungsgemäße Ladephase des Speichersystems. Zusätzlich wurde eine Aussage über deren technische Machbarkeit getroffen.

Zusammenfassend stellt diese Arbeit einen detaillierten Entwurfsprozess des Energiespeichersystems vor. Dieser Designprozess sowie deren Machbarkeitsstudie soll für die weitere Ausarbeitung der Systemintegration dienen.

Schlagwörter: Energiespeicher System, Aluminium-Elektrolytkondensator, DC/DC Leistungswandler, Buck-boost Wandler, Digitaler Regelkreis

Abstract

Power cables play an important role in power grids. Insulation faults in cables can have adverse effects on the operating behaviour. These effects can be assessed through an AC withstand test by using a very-low frequency high voltage generator. This generator produces a sinusoidal voltage waveform at $0.1\mathrm{Hz}$ with high voltage levels up to $65\mathrm{kV}$ peak. During the quality assessment, the power cable is repeatedly charged and discharged. The discharging process is done by a discharging circuit where the energy is dissipated thermally. But to reuse the dissipated energy a novel extension in form of an energy storage system is presented.

This thesis, therefore, describes the design process of an energy storage system that allows the temporary storage of the discharge energy. The developed system is composed of a bidirectional DC/DC converter and an aluminium electrolytic capacitor as storage type. Based on the maximum VLF system ratings the energy storage unit is dimensioned and sized. The effective power flow control between the storage system and the available discharge energy is done by a synchronous buck-boost converter. This bidirectional converter works in continuous conduction mode over the complete charging phase. Together with a theoretical analysis of the underlying problem and the use of converter analysis methods the selected synchronous buck-boost converter is dimensioned and sized. In addition, a state space AC modeling of the converter with its electrical uncertainties is conducted. With the converters AC model, the controller is designed. A closed-loop input converter current control scheme based on a proportional-integral controller is implemented. The system assessment is done by a model-based hardware implementation in Matlab Simulink and Plecs Blockset. The system is rated to store discharge energies up to $4.3\mathrm{kJ}$ in a short charging period of $2.5\mathrm{s}$. The maximum peak power during the charging phase is $2.7\mathrm{kW}$. The digital proportional-integral controller is implemented through an emulation process of the designed analog controller. Based on a C-code implementation of the digital controller the gap between the real hardware is reduced. During the design process theoretical calculations are made and reveal that designing a capacitor storage unit has a direct impact on the peak system currents and also impose also limitations on permissible DC voltage ranges on electrical components. The developed energy storage system and its power flow control strategy were investigated through simulation studies. The results show proper charging of the energy storage medium. In addition, also a statement of the final technical feasibility is made.

In total, this work summarizes a detailed design process of the energy storage system. This proof of concept is intended to further advance the system integration.

Keywords: Energy storage system, aluminium electrolytic capacitor, DC/DC power converter, buck-boost converter, digital control strategy

Contents

1 Introduction

Energy storage systems (ESS) are getting more and more attention in recent years. Through the set of methods and technologies which are nowadays used, different energy forms can be stored intermediately. This allows to access the stored energy at a later time and with the objective of reuse in a purposeful application, whenever it is needed.

One of the prime examples is renewable energy sources, such as wind, solar or photovoltaic. But due to their strong discontinuity in energy production and in some aspects their non-direct use of the available energy, leads exactly to the result that energy storing systems are required [1].

In addition to the above well known example, it should be mentioned that energy can be also available in other various forms as like electricity. For instance, radiation, chemical energy, gravitational potential and kinetic energy are building only a few of other energy sources. These energy sources can be stored in different energy storage types which are classified by their physical acting domain. A recently published review about energy storage types with their applications and recent developments are given in [2].

By using power electronics, the energy transfer for the intermediate ESS can be realized. However, together with the choice of storage type, this still involves several dependencies such as application, system integration, and the availability of the energy source over time. To illustrate the above statement, another commercially widely used principle for energy storage in electric vehicles is presented. Batteries and supercapacitors are frequently used for this purpose. Here, recuperation forms a central mechanism of energy provision. In their function, batteries and supercapacitors form a hybrid storage concept. This hybrid storage concept combines the advantages of both storage types. The electric drive system is used to recover the energy by switching into the generator mode. A bidirectional power converter transfers the provided power flow to the storage type. An overview of the state of the art in recuperation is given in the article [3].

Due to the strong growing attention to energy storage systems in today's technical applications as shown in electric vehicles and smart grid use, various benefits are ensured [2]. On the one hand, the electrical energy losses in electrical systems can be reduced while on the other hand reducing voltage fluctuations, improving power quality and increasing reliability as well as improving energy efficiency are only a few further positive aspects. However, despite all the advantages that an energy storage system brings,

there are some crucial problems such as controllability, changeability, and stability itself of the underlying power and energy demand.

These challenges lead engineers to develop stable energy storage systems that manage power and energy flow in an optimal manner. Generally, an ESS is categorized in a charging and discharging period. The first mentioned charging phase is done whenever energy is realized in any way and means, for example, electrical dissipation energy or kinetic energy during recuperation. The discharge phase is then used primarily in defined, targeted application scenarios to make the stored energy available. Such use cases can be to optimally overcome power peaks shaving or prevent the probability of failure of the device as it is presented in [4].

Based on these initial findings and the dependencies between energy storage topology and power electronics, a closer look will be taken at the stated problem. Based on the conceptual formulation, of the energy storage system which shall be developed a more detailed examination can be performed.

1.1 Statement of the Problem

In order to specifically address the problem of this thesis in concrete terms, a brief insight view of the general situation must be presented. This thesis stays in contact with a diagnostic system called a very-low frequency (VLF) generator, which can be used to assess the insulation quality in power cables. Now, subsequently, a step-by-step introduction to the problem follows. In the first part, the basic mechanisms of the underlying diagnostic system is presented. In further steps then the underlying problem and the transition to the energy storage system are then clarified.

Power cables play an important role in energy distribution networks. The most commonly used cables are XLPE cables [5]. In the meanwhile, insulation failures of cables have become a severe safety hazard. Through the use of a VLF high voltage generator, an AC withstand test can be performed, to assess the quality of the power cable. In Figure 1.1 a simplified structure of a VLF test system with the device under test (DUT) is shown. The specimen under test can be described as a linear model with isolation consisting of a parallel connection between the cable capacitance C_{cable} and a high ohmic insulation resistor R_p. For an ideal cable, R_p is infinite. The quality measurement that is taken is referred to loss factor ($\tan\delta$).

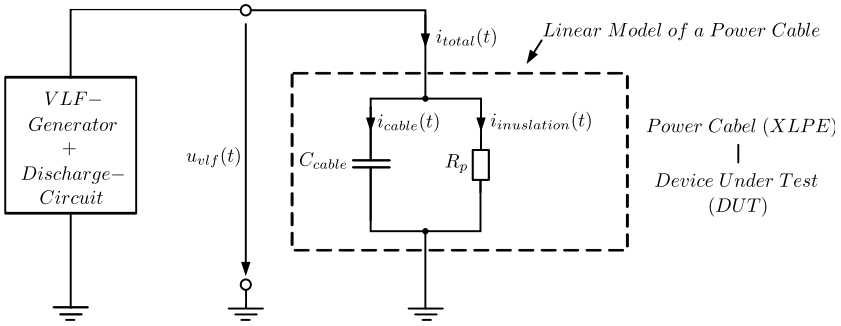

Figure 1.1: Schematic structure of a VLF AC withstand testing application where on the left side the VLF generator is accommodated and on the right side the simple equivalent circuit model of a power cable (DUT) is seen

With the use of the generated VLF sinusoidal waveform (Parameters: $f_{vlf} = 0.1\text{Hz}$) the AC withstand test is carried out. In Figure 1.2 the very-low frequency test voltage $u_{vlf}(t)$ of the generator under ideal power cable conditions is shown. Hereby, the signal curves $u_{vlf}(t)$, $i_{cable}(t)$ and $p_{cable}(t)$ are demonstrated only to reflect the signal characteristics during testing and are therefore not truthfully deposited. The resulting power flow $p_{cable}(t)$ is shown on the left which has the double frequency of $u_{vlf}(t)$.

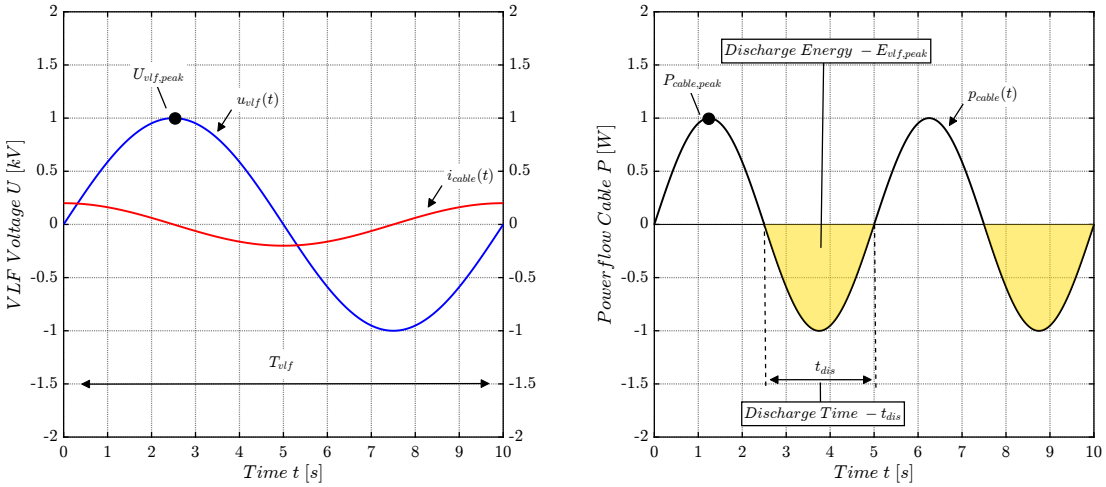

Figure 1.2: Very-low frequency test voltage of a VLF high voltage generator in order to assess the insulation quality $\tan\delta$ of a power cable

It can be recognized that during a measurement period T_{vlf} the system passes two phases, according to its resulting power flow $p_{cable}(t)$. In each half-wave of $u_{vlf}(t)$, the power cable is charged and discharged. The discharge phases of the stored energy can be therefore attributed to quadrants two and four of the VLF sinusoidal voltage. The generator setup consists in its structure of a high voltage cascade ([6]) to produce the VLF test voltage while due to the discharge phase a discharging circuit is necessary. By decoupling the charging and discharging phase, the discharge energy can be separately thermally dissipated. The evaluation of the $\tan\delta$ is then done after each VLF period. Due to cable aging, for instance, insulation faults happen. This affects the insulation resistance and causes a reduction, whereby an insulation current $i_{insulation}(t)$

is flowing. This leads to a deterioration of the loss factor and severe hazard situations are the consequence. A graphical representation of a phase diagram chart shows the differences between an ideal and nonideal cable, in which the $\tan\delta$ as the meaningful quantity to describe the cable quality is illustrated [7].

Using the aforementioned explanations on the VLF generator subject and their measurement principle in assessing the insulation quality the idea of energy recuperation was born.

In terms of energy recuperation, the idea is created to utilize the discharge energy $E_{vlf,peak}$ in such a way that it can be stored in an intermediate circuit. Concerning the stated problem a technical investigation has to be made. A model-based hardware implementation for giving the first proof of concept for an energy storage system in a very-low frequency high voltage generator application shall be developed.

The fundamental consideration for this investigation focuses on Figure 1.2. It can be remarked that during one measurement period T_{vlf} two discharging phases with the duration $t_{dis.} = 2.5\mathrm{s}$ are present. The provided discharge energy which is covered in yellow in quadrants two and four of the sine wave $u_{vlf}(t)$ has to be stored.

The maximum discharge energy $E_{vlf,peak}$ is therefore directly related to the square of the applied voltage since the power cable can be represented as a capacitor. This relation is quantified by the following Equation 1.1.

$$E = \frac{1}{2} \cdot C \cdot U^2 \tag{1.1}$$

The maximum achieved power ratings of the VLF test system are listed in Table 1.1 and have been provided by the company Baur GmbH. These performance data are used throughout the whole thesis as boundary conditions for the design process. The maximum discharge energy is calculated by formula 1.1 and is the main parameter on which the storage type depends. The discharge time is defined as a quarter of the VLF period time T_{vlf}.

Additionally, during a normal VLF test procedure, ten periods are driven to investigate the tangents delta ($\tan\delta$) factor. This procedure is done with different RMS VLF voltage values. If further information about field testing of power cable systems using very-low frequency high voltage signals, the IEEE standard 400.2 is recommended.

So in conclusion the idea was born to develop an energy storage system that intends to functional short-term energy storage system. With regard to the VLF generator, several manipulated variables in the overall VLF system are neglected because of their high complexity. The energy storage system is developed in cooperation with the company Baur GmbH in Sulz. In the first instance, only the charging phase should be defined.

Table 1.1: Maximum performance data of the VLF test system under AC withstand testing

Symbol	Meaning	Value	Unit
$U_{vlf,peak}$	Peak Voltage VLF Generator	65	$[\mathrm{kV}]$
f_{vlf}	VLF Frequency	0.1	$[\mathrm{Hz}]$
T_{vlf}	VLF Period	10	$[\mathrm{s}]$
C_{cable}	Maximum Capacitance Power Cable (DUT)	2	$[\mu\mathrm{F}]$
$P_{cable,peak}$	Peak Power	≈ 2.7	$[\mathrm{kW}]$
t_{dis}	Discharge Time	2.5	$[\mathrm{s}]$
$E_{vlf,peak}$	Maximum Discharge Energy	4225	$[\mathrm{J}]$

1.2 Motivation

As it is described in Subsection 1.1 an energy storage system for a VLF generator shall be developed. The challenge of the system lies in definitely finding the right energy storage type. In particular, this involves transferring the electrical quantity of electricity into manageable orders of magnitude. The underlying peak power of $2.7\mathrm{kW}$ and a short-time energy quantity of $4225\mathrm{J}$ make this task particularly challenging. The interaction of discharge energy and a controlled transfer of the energy flow through a suitable power converter is challenging too. The phased requirements of enabling energy storage with concern of power flow controllability and stability issues will also find their accusation. Based on this, the fundamental question lies in the feasibility of such a system. A concept must be created based on targeted requirements. The question of additional safety concepts and the feed-in after the charging phase are further aspects that can be taken into account in such a system integration. Another question that arises in such an application is the choice of energy storage type. In the applications which are presented in the introduction chapter, one or two common features can be identified when comparing the stated problem with the electrical vehicle utilization. With a first interpretation of the charging phase development, a first statement can be made about whether such high energy storage amounts are possible to store technically.

The motivation of this thesis shall lie in developing a system design concept that should present a proof of concept in terms of a technical manner.

1.3 State of the Art

In Chapter 1, an introduction has already been made in which two energy storage system applications are presented.

This section will provide a short review of some technical implementations of ESS.

One type of energy storage is used in an electrical tram system in public transport [4]. Through the use of an On-Board-Energy-Storage-Device (OBESD) which consists of a super-capacitor bank and lithium-ion battery, power dispatcher operation modes like accelerating and moving the tram can be improved. During dwelling at a station, the capacitor bank is connected directly over the contact line to a DC bus. With the use of a bidirectional converter, the capacitor can be charged up again while in later use the lithium-ion battery can be charged.

Another prominent application of an energy storage system is the use of a bidirectional DC/DC converter for incorporating regenerative braking energy. A well-known system in that field of application is the Kinetic-Energy-Recovery-System (KERS) in Formula one cars. Through the use of power electronic methodology, the current power flow of regenerative breaking energy can be absorbed by a supercapacitor bank. The braking energy is stored temporarily in a supercapacitor bank via an intelligent energy conversion network which is comprised of an electric motor and a power electronic unit. The electric drive system is the key element in which kinetic energy is converted to electrical energy. The system charges up the supercapacitor under breaking manoeuvrer and is releasing the same amount of energy under acceleration [8].

A further form and a slightly different form of an energy storage application is presented by Liebherr-Werk GmbH [9], and is called Pactronic. This hybrid power drive concept presents a new millstone for mobile harbour cranes. The system is characterized by a hydraulic energy storage device. The potential energy in this case is stored in an accumulator and can be released on demand. The charging of the accumulator is done by regenerating the reverse power while lowering the load. This system increases the overall efficiency.

All the energy storage technologies which are presented have something in common, namely their structure. In many technologies, a power conversion system and an energy storage type are used. The choice of the energy storage device depends crucially on the application and area of use. The power conversion system is in many utilizations built up to allow a bidirectional power flow. In this short state-of-the-art review, it becomes clear that bidirectional converters together with the energy storage device are the key components. Through the bi-directionality of the converter, the energy storage system enables a flexible power processing interface between the energy saving system and the rest of the system.

1.4 Objectives of this Thesis

Inspired by the aforementioned state-of-the-art technologies, which are mostly based on power converter systems and different energy storage types an ESS shall be developed. This thesis aims to present a proof of concept to solve the stated problem, for allowing a technically feasible short-term energy storage system use. The proof of concept shall contain, in the first aspect a design scheme while secondly a final model-based digital controlled hardware implementation on a simulation basis, in Matlab Simulink and Plecs Blockset shall be done. It shall give a closer design insight into which way such large short time-based energy amounts can be technically stored. The cornerstones of this work are definitely the controllability of the power flow from the primary side of the ESS to the secondary side of the storage medium. According to the described technologies in 1.3, the selection of the energy storage type is an enormously important matter and depends mainly on the application and how the energy is available. This work shall therefore investigate different energy storage variants in order to filter out their advantages and disadvantages for the best use case for the stated problem. A technical-based assessment study on a simulation basis with the final digital controlled developed hardware implemented ESS shall be conducted. In this assessment, the current ratings and voltage ratings around and during the charging process shall be verified with respect to controllability and their compliance with electrical component limits. Based on this feasibility study on the subject of energy recuperation in VLF generator systems, it shall be possible to clarify further aspects. This can, for example, be concerning the execution of the system integration, where it still has to be clarified in which way the stored energy is used in later time stamps during the AC withstand test.

1.5 System Requirements

Based on the explained problem description in Section 1.1 and the analysis of the state-of-the-art energy storage systems in Section 1.3, a requirement profile could be created in cooperation with the company Baur GmbH.

In this section, a detailed requirement list for the energy storage system is derived to fulfil functionality, electrical parameters, software and energy efficiency. Outgoing from these framework conditions, a concept can be developed to characterize the functionality by a model-based hardware simulation.

The requirements are listed specifically for the respective system groups called

- Energy Storage Type and the
- Power Converter Topology.

For each group a specific requirement profile is given, which will be presented in Subsection 1.5.1 and 1.5.2. A distinction between a selectable, a mandatory and a requirement itself is made. A selectable requirement has the meaning that a dependency on other requirements is given.

1.5.1 Requirements Energy Storage Type

In Table 1.2 the requirements for the energy storage type are listed. It has to be noticed that in terms regarding to a final product design, cost points and volume points are not to be taken into account. The main goal is still in getting the first proof of concept.

Table 1.2: Specification list for the energy storage type

Symbol	Meaning	Value	Unit	Type
$E_{vlf,peak}$	Maximum stored energy	≈ 4225	$[\mathrm{J}]$	Requirement
t_{ch}/t_{dis}	Charge-/ Discharge-time	2.5	$[\mathrm{s}]$	Requirement
n	Lifetime (cycles)	> 10000	$[\,]$	Mandatory
C_s	Storage Capacity	x	$[\mathrm{F}]$	Selectable
U_s	Rated Voltage Storage Capacity	400	$[\mathrm{V}]$	Mandatory
P_{spec}	Power density	x	$[\mathrm{kW/m^3}]$	Not Mandatory
E_{spec}	Energy density	x	$[\mathrm{Wh/kg}]$	Not Mandatory
μ_s	Storage type cycle efficiency	$> 90\%$	$[\%]$	Mandatory
ΔU_s	Minimum / Maximum charging voltage level	60 - 350	$[\mathrm{V}]$	Mandatory

Based on the requirements list, it is clear that electric and electrochemical energy storage systems will be the choice. The storage capacity C_s is selectable. This means that the capacity of the storage system is depending on the amount of energy $(E_{vlf,peak})$ that must be stored in one charging process and which voltage difference can be exploited. Charge and discharge time are of significant importance since the overall charge and discharge time are given by a quarter of a full very-low frequency period T_{vlf}. A minimum and maximum voltage variability ΔU_s must be given by the storage process to guide the power flow during the discharge phase into reasonable current ranges. The rated voltage affects the energy acquisition and is coupled in the same way as with the minimum and maximum charging voltage to the discharging power flow. The lifetime properties shall guarantee low maintenance of the energy storage device. Effects like temperature changes and aging of the capacitor are in most cases responsible for capacity losses and can be further investigated in Literature [10].

1.5.2 Requirements Converter Topology

The second respective system group is defined as the power converter topology. There are many different types of converters available for different application scenarios [11]. It is therefore vital to get a decision on a specific topology to achieve the desired result. The converter system proposes the management system of power flow between the primary and secondary side of the energy storage system. Thereby, this system forms a power flow control mode that appropriately transfers the power. In Table 1.3 the necessary requirements for the power flow converter are listed. It has to be remarked, that requirements are categorized as desired once, mandatory and requirements themselves. A requirement is specified with a quantity which is measurable like for example the inductor current $i_L(t)$.

Table 1.3: Specification list for converter topology

Symbol	Meaning	Value	Unit	Type
-	Step-up Step-down Ability	-	x	Mandatory
-	Bidirectional	-	x	Desired
Δi_L	Inductor Ripple Current	20	$[\%]$	Requirement
f_{sw}	Switching Frequency	50	$[\mathrm{kHz}]$	Requirement
$U_{in,min}$	Minimum Input Voltage	$[\mathrm{V}]$	100	Requirement
$U_{in,max}$	Maximum Input Voltage	1100	$[\mathrm{V}]$	Requirement
CCM	Conduction Mode	-	-	Mandatory
$I_{L,ave}$	Average Inductor Current	$15-20$	$[\mathrm{A}]$	Requirement
-	Galvanic Isolation	-	-	Not mandatory

Step-up and Step-down Ability

The converter shall have the capability of stepping up and stepping down the input voltage. Depending on the input voltage on the primary side and the rated power flow it is necessary to provide both functional features. This improves the variability of the power flow control process.

Bidirectional Converter

In diverse applications, bidirectional power flow DC/DC converters are increasingly employed. In the case of a bidirectional converter sizing and additional components can be reduced to a minimum, due to the fact that the system can operate forward and reverse power flow direction. Furthermore, bidirectional DC/DC converters are one of

the key elements in electrical energy storage systems [11].

Converter Design Specifications
Further design specifications are the inductor ripple current Δi_L. The inductor defines the energy storing element which transfers electrical energy in specific power flow time stamps to the energy storage type. This causes an indirect effect from the inductor to the output current ripple. So in this way, the system shall operate in continuous conduction mode with an inductor current ripple which is specified by 20% of the maximum mean inductor current $I_{L,ave,max}$. By means of the inductor current, the continuous conduction mode CCM shall be implemented. The difference between the continuous conduction mode (CCM) and the discontinuous conduction mode (DCM) of a converter is given by the inductance current characteristics. The CCM is defined to decrease the inductor current ripple in comparison to the DCM. A detailed description of the different conduction modes can be found in [12]. The switching frequency f_{sw} is set with $50\mathrm{kHz}$, this shall reduce switching losses since high power flows are expected. An appropriate reason for galvanic isolation is not specified. The input voltage and output voltage can share their common ground.

Based on this framework, a conceptual study can be conducted. According to the listed requirements from Section 1.5, the investigation for the desired system design can be made. The technical feasibility shall be in the foreground. The costs and volume points are considered as further optimization points in the second phase of the development process.

1.6 Structure of the Thesis

The structure of this thesis is based on a concept decision phase followed by a detailed system design process and a final system verification. In the conception phase, suitable storage technologies and converter topologies are evaluated. Each system group presents possible solutions to fulfill the requirements. Afterwards, the presented solutions are then independently evaluated through a utility analysis based on evaluation criteria. The solution with the highest overall score is then used for the further system design. In the following chapters afterwards, the system design process as well as its model-based hardware implementation is shown. The system design process forms recurring dependencies between different system groups as well as a calculation that is highly dependent on theory. Finally, the energy storage system is evaluated and verified to obtain a statement about its feasibility.

2 Concept

According to the stated problem in Section 1.1 the conceptual design phase is divided into two major subgroups, called energy storage type and converter topology. In this chapter, the first part concentrates on defining and selecting an appropriate choice of an energy storage device according to the requirements in Subsection 1.5.1. In the second half, suitable converter topologies are analyzed and evaluated with regard to the requirements from Subsection 1.5.2. Based on a utility analysis the most promising topology is used.

2.1 Selection of Suitable Energy Storage

To ensure the mechanism of storing energy from the VLF power path, a suitable storage device is required.

For this purpose, the Ragone diagram in Figure 2.1 is primarily used as a visualization for comparing different energy storage technologies. The Ragone diagram presents the storage device energy density versus the power density on a double logarithmic representation. The main diagonals in this figure illustrates the charging and discharging times [13], [14].

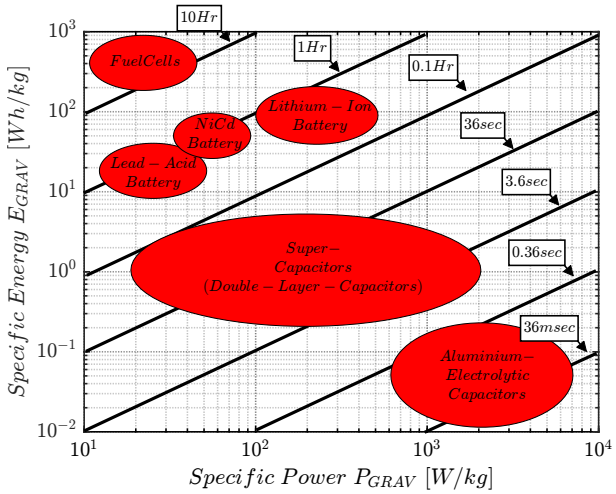

Figure 2.1: Incorporation of energy storage devices in the Ragone diagram reproduced from [2]

With the use of the Ragone diagram a better thorough understanding of the energy

storage type can be given in terms of power and energy ratings, as well as charge and discharge times.

To reduce the choice of energy storage types, only electrochemical and electrical storage variants are elaborated in this context, since the available energy is of electrical quantity. In a more detailed analysis of the presented Ragone diagram and under consideration of the storage requirements from Subsection 1.5.1, it can be seen that due to long charge and discharge times, batteries are out of specification and therefore they are not suitable for the desired application. This leads ongoing to an extensive elaboration on aluminium electrolytic capacitors and supercapacitors. According to the following evaluation criteria in Subsection 2.1.1 the elaboration of aluminium electrolytic capacitors and supercapacitors is conducted. Through a final utility analysis, the most promising storage device is chosen for further system design.

2.1.1 Evaluation Criteria

With the aid of the below-listed evaluation criteria, the supercapacitor and aluminium electrolytic capacitor storage variants are investigated. These evaluation criteria shall help to meet the appropriate storage system choice.

- **Charge- / discharge time:** The requirements show that a high amount of energy must be absorbed by the energy storage system in a short period of time. Short and fast charging and discharging times are preferable.
- **Charge / discharge cycles:** During charge and discharge periods complex reactions happen. In batteries for example chemical reactions are caused due to charge and discharge procedures. This can give an impact on the performance and can minimize energy storage capacity [10]. During an AC-Withstand test with a VLF system, many charging and discharging cycles are expected.
- **Lifetime:** The number of charge and discharge cycles as well as temperature dependency influence the lifetime of the storage system and can cause a reduction of the capacity.
- **Power density:** Describes the energy transfer rate per unit volume or mass of an energy storage system.
- **Energy density:** Describes the energy which is accumulated per unit volume or mass.
- **Rated Voltage:** The rated voltage criteria define the voltage variability of an electrical energy storage device. Due to the expected high power ratings of $2.7\mathrm{kW}$ during the power cables discharge phase an increased voltage variation is preferred.
- **Equivalent Series Resistor (R_{ESR}):** The serial equivalent internal resistance $R_{ESR,C}$ determine the self-heating of the energy storage device. A small ESR is also preferable here in order to lower dissipation losses.

In the following Subsections 2.1.2 and 2.1.3, the analysis of those storage systems that have been identified as shortlisted is performed.

2.1.2 Aluminium Electrolytic Capacitor

AS one of the most direct ways of storing electrical energy is done by using capacitors. Typical capacitors are aluminium electrolytic capacitors (AEC), ceramic capacitors and tantalum capacitors. These types of capacitors collect and store charges on the plane electrodes.

The capacitance of typical capacitors is built up through two plane electrodes which are isolated through a dielectric material. So in this case capacitance values are ranging from single micro farad up to milli farads. In comparison to supercapacitors their capacitance per unit volume is much lower but their rated operating voltages are around 300 times greater. Especially in applications where the total capacitance is in the medium capacitance range and the rated voltage has to be in a higher volt range makes them suitable for it.

The charge and discharge times of conventional capacitors are typically in the range of picoseconds to milliseconds, while the charge times of super capacitors are in the range of milliseconds to seconds with Reference to [14]. In comparison, batteries have a lower charging power compared to capacitors, which leads to a longer charging time. Due to their high energy density, batteries are able to supply energy over a longer period of time instead of conventional capacitors. Capacities, however, provide a high power density in short time periods.

The charge and discharge capability of conventional capacitors and supercapacitors ranges around a million cycle life states. With regard to this assertion, batteries are reduced in their cycle life by a factor of about 250 compared to capacitors. Another measurement that is directly associated with the charge and discharge process is the resulting efficiency. The overall charge/discharge efficiency for a conventional capacitor ranges at around 95 $\%$, while batteries have values in the range of 70 to 85 $\%$, with accordance to [15].

In comparison to supercapacitors, aluminium electrolytic capacitors have cell voltages that are 300 times greater. In this case, no worries about equalization circuits for voltage balancing of a capacitor module have been taken into account. This reduces the circuitry effort tremendously and makes them easier to install.

Another important aspect is the operating temperature range capability. Typical charging temperatures for conventional capacitors are ranging from -20° to 125°. Supercapacitors temperature range is on the magnitude base of -40° to approximately 65°. Due to the equivalent series resistor, additional energy losses contribute to the system and affect the internal temperature. A better inside view of this subject gives the equivalent circuit model of a capacitor in Figure 2.2. This simplified model represents a first-order

circuit model, which consists of four circuit components. In the current consideration, the inductance L is neglected because it is usually small. During the charging and discharging processes the equivalent series resistance (ESR) $R_{ESR,C}$ contributes mainly to the energy losses ($P_{loss,C} = I^2 \cdot R_{ESR,C}$) and in further consequence a temperature rise occurs.

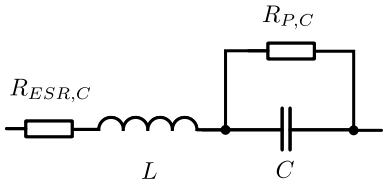

Figure 2.2: First-order equivalent circuit model of a conventional capacitor

The parallel Resistor on the other side $R_{P,C}$ simulates mainly those energy losses due to self-discharging. This resistor is also often referred to as the leakage current resistance. So in a real capacitor, the Resistor $R_{P,C}$ is always much greater than the $R_{ESR,C}$. In a typical energy storage application, capacitors as an energy storage system are connected in series or in parallel to build up a module in order to fulfill the design requirements.

In Equation 3.4 the total capacitance C_{Total} and the total equivalent series resistance R_{Total} of the designed storage capacitor module is given.

$$C_{Total} = C_{cell} \cdot \frac{m}{n} \qquad R_{Total} = R_{Cell} \cdot \frac{n}{m} \tag{2.1}$$

The abbreviations n and m describe the number of series cells and the number of branches that must be in parallel connection. C_{Cell} and R_{Cell} represent the total capacitance and equivalent resistor of the capacitor storage bank. Besides the power losses explanation that occurs a time-based characteristic quantity is derived. The response time constant ($\tau_C = R_{ESR,C} \cdot C$) in an aluminium electrolytic capacitor is about $\approxeq 10^{-4}$ whereas in supercapacitor usually a longer response has to be expected. For further information about parasitic model parameter extraction on capacitors as well as an expanded side-by-side energy storage technology comparison, it can be referenced on [16].

2.1.3 Supercapacitor

In addition to the Ragone diagram in Section 2.1, it can be stated that supercapacitors are placed in terms of energy and power density between batteries and conventional capacitors. Supercapacitors are also known under vernacular names such as power capacitors, electrochemical-double-layer capacitors (EDLC) or ultracapacitors (UCaps). These storage types feature long life, high power capabilities and have capacitances of several order of magnitude, due to their internal structure [17]. In this

way these capacitors are also referred as electrochemical capacitors which make them similar to batteries. A further description of the internal structure can be found in Literature [14], where also a comparison review against aluminium electrolytic capacitor is presented.

Supercapacitors are nowadays available in sizes up to several hundred farads per unit but only have voltage ratings of 2.3 to 3.3 V per cell. In terms of their functionality supercapacitors are governed by the same principels as conventional capacitors. The only difference are in their internal structure. A much higher surface area and their thinner dielectric material provide high capacitance[18].

Their ability to be charged and discharged in a matter of a few seconds determines the feasibility of their use in a particular application like [4]. With these characteristic time properties, fast recharging can be managed. Additionally, the power delivery is 10 to 25 magnitudes greater, than compared to batteries [19]. For further actual review information about important features and limitations of batteries, supercapacitors and conventional capacitors, Table 1 in Literature [2] is recommended. Always depending on the internal structure of the supercapacitor, or double-layer capacitors offer an energy density that is 10 to 100 times bigger than conventional capacitors.

In comparison to lithium-ion batteries, supercapacitors point out by long cycle life, in the magnitude of order 500 times higher. Directly compared to conventional capacitors no major quantity difference is given between these two topologies. The cycle life as mentioned before is also affected by the temperature. In UCaps and conventional capacitors these temperature ranges are defined, in accordance to Literature [2] between the range of -40 to $70°\mathrm{C}$ and -20 to $125°\mathrm{C}$, whereas in batteries temperatures of 0 to $45°\mathrm{C}$ are normal during charging.

To guarantee an adequate life expectancy of a supercacpacitor module, active or passive balancing circuits have to be considered to minimize differences in cell voltages. Especially care must be taken when ultracapacitors are connected in a string since each individual cell cannot exceed the maximum proposed cell voltage. In a further consequence, this can lead to permanent damage. In Literature [19] a comprehensive review on supercapacitor and their applications and developments as well as equalization circuit strategies are presented and explained in a much more detailed fashion.

In Table 2.1 a useful comparison between an ultracapacitor with a representative lithium-ion cell and an aluminium electrolytic capacitor is done to get a better inside into all those mentioned characteristic quantities.

Table 2.1: Comparison of ultracapacitor with lithium-ion cell and aluminium electrolytic capacitor

Attribute	Ultracapacitor BCAP0350	Lithium-Ion 18650 cell	Aluminium-Electrolytic-Capacitor ALS71H203QT400
Capacitance	$350\mathrm{F}$	$2.1\mathrm{A\,h}$	$20\mathrm{mF}$
Voltage	$2.7\mathrm{V}$	$3.6\mathrm{V}$	$400\mathrm{V}$
Resistance	$3.2\mathrm{m\Omega}$	$75\mathrm{m\Omega}$	$12\mathrm{m\Omega}$
Mass	$63\mathrm{g}$	$70\mathrm{g}$	$2\mathrm{kg}$
Volume	$5.3e^{-5}\mathrm{m}^3$	$1.7\mathrm{m}^3$	$5.5e^{-3}\mathrm{m}^3$
Cycles	> 500000	< 2000	> 500000
Peak Energy	$E_{UC} = \frac{C \cdot U^2}{7200}$	$E_{Li} = C \cdot U_{OC}$	$E_{AEC} = \frac{C \cdot U^2}{7200}$
Peak Power	$P_{pk} = \frac{U^2}{4 \cdot R_{ESR,C}}$	$P_{pk} = \frac{2 \cdot U_{OC}^2}{9 \cdot R_{int}}$	$P_{pk} = \frac{U^2}{10 \cdot R_{ESR,C}}$
Peak Power P_{pk}	$569.53\mathrm{W}$	$38.4\mathrm{W}$	$1.3e^{6}\mathrm{W}$
Peak Energy E_{pk}	$0.354\mathrm{W\,h}$	$7.56\mathrm{W\,h}$	$0.222\mathrm{W\,h}$
Specific Energy Density	$5.62\mathrm{Wh/kg}$	$108\mathrm{Wh/kg}$	$0.11\mathrm{Wh/kg}$
Charge Temperature Range	-40 to $65^\circ\mathrm{C}$	0 to $45^\circ\mathrm{C}$	-40 to $85^\circ\mathrm{C}$

2.2 Utility Analysis

In the previous Section 2.1, suitable storage topologies are presented. The selection of these storage topologies results from the need to achieve fast charging and discharging times and to meet the requirements to temporarily store the discharged energy over a defined voltage range. This section compares finally the presented topologies. In Table 2.2 the utility analysis is shown. In the utility analysis, points are awarded from one to ten. Even though batteries were initially excluded, it was decided to include them in the evaluation as well to significantly show the differences.

Table 2.2: Comparison of the presented electrical storage topologies

Storage Topologies	Rated Cell Capacitance C [F]	Rated Cell Voltage U_{Cell} [V]	Charge-Discharge-Times $t_{c,dc}$ [s]	Charge-Discharge-Cycles n [ ]	Temperature Range ΔT [K]	Peripherals	Total Points
Batterie LI-Ion	1	3	1	3	6	2	16
Aluminium-Electrolytic-Capacitors	4	8	9	9	7	7	44
Supercapacitors	10	3	7	9	6	5	40

The result of the utility analysis shows that the aluminum electrolytic variant is the most suitable form of energy storage. With regard to the aluminium electrolytic capacitor and its rated capacitance and the rated cell voltage (compared to the supercapacitor) an overall higher score is reached than compared to the super capacitors. The low effort of cell balancing techniques and their fast charge and discharge times affirm them as a suitable choice for the desired power application.

For the remaining topologies like supercapacitors and batteries, no further investigation has to be made. In comparison to the charge and discharge cycles of the supercapacitors lower cycle lifes will be achieved with batteries. Furthermore, long charge and discharge times do not make them an appropriate choice of use, since the energy storage has to be done in less than three seconds, as it is mentioned in Section 1.1.

With a further look at the power and energy transmission, the supercapacitor variant can be a promising alternative too. However, a certain voltage variability must be present in the case of providing manageable charging currents. Finally, the converter topology has to be able to handle the charging currents. Another major drawback behind supercapacitors is their series composed module structure to generate higher total voltage ratings.

Based on this utility analysis, the aluminium electrolytic capacitor variant will be further considered in the system design process.

2.2.1 Summary Energy Storage System

In this section, the most promising concept was selected from the three electrical storage topologies, which are evaluated by using evaluation criteria. It was specifically stated that due to changing energy forms additional losses occurs, and only those storage technologies are to be considered that work in the electrical domain. So in that case, the most important properties of the electrical and electrochemical storage topologies are compared against each other by using the Ragone diagram. Subsequently, then the energy storage topologies are explained with respect to rated capacitance, rated operating voltage, charge and discharge times and other characteristic quantities. After that, based on the system requirements and the aim of a predevelopment, the storage systems are utilized against each other. It must be noticed, that this concept phase does not consider cost points and volume points. Through the defined energy storage system a first design of the storage system can be made. In the further course of the concept phase, the appropriate converter topology is identified.

2.3 Selection of a DC/DC Converter Topology

Various DC/DC converters with interleaved technology or bidirectional capability are getting more and more attention [20]. Especially bidirectional converters are a preferred choice in energy storage systems. With regard to this, they provide the ability to control the power flow in either forward or backward directions.

In this section, various possible circuit topologies will be examined and compared with each other. On the basis of evaluation criteria, the most promising concept is chosen. Based on the choice of the circuit topology, the system design is carried out.

With the assistance of the converter requirements from Subsection 1.5.2 following important aspects must be considered to narrow the search for power converters:

- **Topology:**
  Due to the specification that the input voltage is not constant and drops during the discharge phase similar to a quarter period of a sinusoidal voltage, the converter must operate as a step-down or step-up converter, depending on the charging voltage at the energy storage device. For this reason, a converter with the ability to stepping-up and stepping-out have to be preferred.
- **Galvanic Isolation:**
  Galvanic insulation is not mandatory. Non-isolated DC/DC converters are the preferred choice of us because it allows current flow directly from input to output. This reduces complexity, size and price.
- **Operation mode:**
  The converter shall operate in continuous conduction mode (CCM) throughout the discharge cycle. During this switching mode, the converter has to be capable to work as a buck, boost or a buck-boost converter.
- **Transmission Rate:**
  The minimum and maximum transmission ratios of the converter shall not be exceeded. Instability issues during power flow conversion due to oscillation have to be avoided. The actuating variables (duty cycle) are limited to the lower 5% and the upper 95% of the duty cycle.

2.3.1 Evaluation Criteria DC/DC Converter

In order to finally enable a comparison between suitable topologies, evaluation criteria have to be defined. Assessments regarding assemblies volume of the converter topology are not considered. The aim of the evaluation is to find a circuit variant for the depicted problem from Section 1.1. The objectives are to fulfill the requirements from Subsection1.5.2. The main criteria are therefore the ability to drive the power converter in buck, boost or mandatory in buck-boost mode. The following list presents the evaluation criteria:

- **Amount of components:**
  The main objective is to solve electrical issues with less components. This reduces complexity, and bulkiness and allows a simpler circuit design. Especially the number of components for the power section, as for instance the number of inductors, transformers, switches or diodes significantly determine the topology and characteristics of the converter.
- **Operationability:**
  Operability defines whether it is possible to work in different conversion directions. That means, is the underlying topology able to work in Buck, Boost or Buck-Boost mode depending on the input and output voltage condition.
- **Industrialization:**
  Under this criterion, the technical feasibility of the converter topology should be considered. Those topologies that have proven themselves in various applications are to be preferred.
- **Peripherie:**
  This evaluation criterion shall take into account the additional effort which must be taken to drive the semiconductor circuits effectively.
- **Voltage at the switches:**
  The occurring voltage at the semiconductor switches has a direct effect on the losses. It follows that the semiconductor switches must have a certain electric strength. The total losses of the semiconductor during switching on and off must be analyzed.

In the next Subsections 2.3.2, 2.3.3 and 2.3.4 suitable converter topologies are presented.

2.3.2 Synchronous Buck-Boost Converter

In Figure 2.3 the circuit topology for a synchronous buck-boost converter is illustrated. This figure represents two combined converter types: On the hand, the buck converter is presented and on the other hand the boost converter. This converter topology has already been discussed and explained in detail in various technical Literature [21], [20]. For this reason, a detailed description will not be given and only a summary of the most important findings from the literature will be presented.

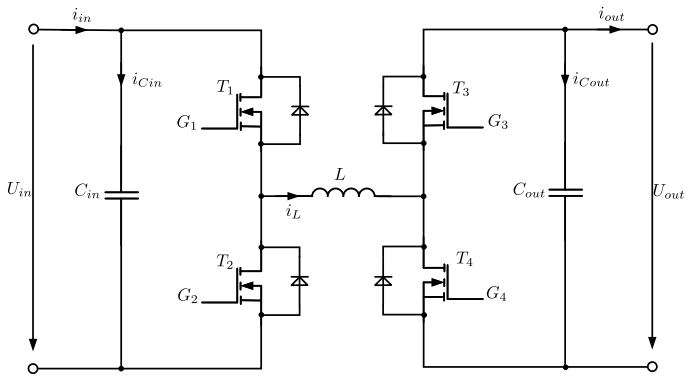

Figure 2.3: Circuit topology of a synchronous buck-boost converter in a H-Bridge configuration

This topology is derived from the non-inverting buck-boost converter. It is built up symmetrically. As explained, the circuit topology is achieved through a cascaded arrangement of a buck and boost converter. The representative diodes of the non-inverting buck-boost topology are replaced through active switching elements. With this replacement, a 4-quadrant operation technique is possible and hence this topology allows energy flow in both directions. Due to this bidirectional power flow is enabled. The buck-boost is implemented in an H-Bridge topology and has an adaptive architecture where it can operate in one of the three modes called a buck, boost or a buck-boost depending on the input to output voltage ratio. In Literature [22] a table of the switching states of the MOSFET switches T_1, T_2, T_3 and T_4 is shown to execute the different converter modes.

In its H-Bridge configuration, the synchronous buck-boost converter only requires one single inductor L. Some advantages are that less passive components are in use, high flexibility is guaranteed and high efficiency in high and low power conversion areas can be given.

All in all, this makes the system most versatile but also brings drawbacks with it. One of the major drawbacks is definitely the number of switches, which affects switching losses. More complexer control algorithms and more turn-on losses because of reverse recovery problems of the transistors body diodes will also occur. In the case of the use of NMOS transistors as high-side switches, a charge pump is needed. Through this, a sufficient gate drive voltage has to be established. As a consequence, this makes the control system and control algorithm of the semiconductor switches somehow complex.

The use of a half-bridge driver with internal bootstrapping allows the control of the high-side MOSFET. A further opportunity for reducing the effects of this problem is to use transistors with low gate-source voltage threshold values. For more investigations concerning the integration of NMOS technology in a H-Bridge the above literature is recommended.

Furthermore, it can be stated that this topology uses only one inductor to transfer energy from the primary side to the secondary side. This results in higher efficiency when compared with a combined half-bridge converter (CHB) [23].

2.3.3 Cuk - Converter

The Cuk converter topology is presented in Figure 2.4. The key elements in this circuit are the two inductors L_1 and L_2 at the input and output.

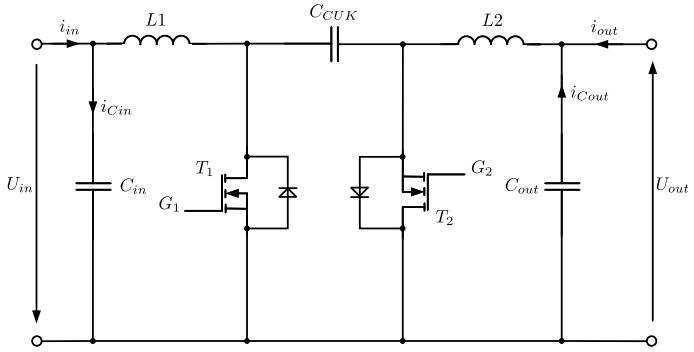

Figure 2.4: Circuit topology of a bidirectional Cuk-Converter

Detailed explanations of this topology can be found in [21], [1], [24], [25]. The findings are presented in the description below.

The bidirectional Cuk is derived from the unidirectional Cuk converter by replacing its diode through a power MOSFET. In its configuration, it inverts the output voltage and can either increase or decrease the input voltage U_{in}. By slightly adjustments of the inductors L_1 and L_2 very small input and output current ripple can be achieved. This is a significant advantage over other inverting topologies such as flyback converter and buck-boost converter. By winding both inductors on the same core the Cuk converter can be optimized in size and considerably eases the requirement profile. Another advantage of this circuit is the straightforward control of the semiconductors T_1 and T_2, where only simple drive circuits due to the low-side MOSFETs can be used. In the same way, as with all converter types, the inductance is used as an energy storage element during the switching phases. The conversion ratio M_{CUK} can vary between the ranges of minus infinity and zero. Additionally, the Cuk converter is inherently unstable when the output current is controlled. If the input current is uncontrolled this can lead to an undamped oscillation between L_1 and C_1. This results than in excessively high voltages across C_1. In order to prevent these oscillations, an additional damping circuit has to be applied. Another disadvantage is that more reactive components are in use. Furthermore, the C_{cuk} couple capacitance have to be greater than the input voltage, which provides a limitation in choice . All in all this converter topology is suited for applications like battery equalization, hybrid supercapacitor batterie interfaces and bidirectional power flow management systems [26].

2.3.4 Sepic - Converter

Basically, this topology from Figure 2.5 is called Sepic converter, which looks quite similar to the above mentioned Cuk converter. The only difference is that MOSFET T_2 and inductor L_2 are rearranged. This converter topology has already been investigated in the Literature [27], [28]. The findings are presented below.

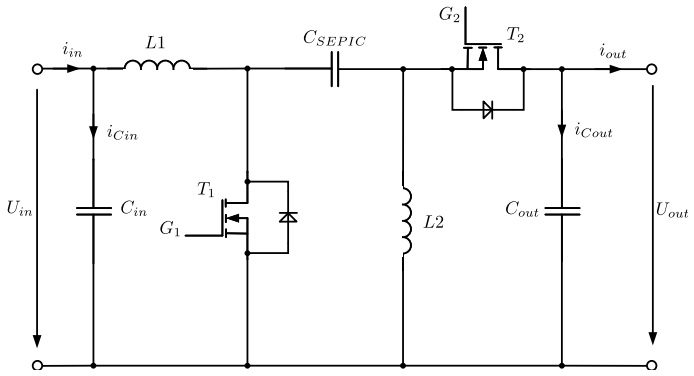

Figure 2.5: Circuit topology of a bidirectional Sepic/Zeta-Converter

The Sepic converter is a buck-boost converter type. This topology includes two power switch (T_1, T_2), two inductors (L_1, L_2) and two capacitors (C_{SEPIC}, C_{out}). The unidirectional Sepic converter can be converted to a bidirectional Sepic converter by replacing the unidirectional switch with a bidirectional switch called MOSFET. Also here the inductors $L1$ and $L2$ can be coupled in order to reduce current ripple, voltage ripple and therefore the voltage stress on the switches. Through the rearrangement of the aforementioned components the Sepic converter obtain a positive output voltage. In theory, the conversion ratio M_{SEPIC} can vary between zero and infinity.

The coupling capacitor has the functionality of blocking any DC current path between input and output lines. Besides this, an adverse effect is definitely the more complex and therefore more vulnerable control of switch T_2 compared to the Cuk converter. Another drawback is that especially the C_{SEPIC} capacitance must have DC voltage ratings that is greater then the maximum input voltage. The dimension of L_1 and L_2 can be chosen to be equal. Moreover, ceramic capacitors are the preferred choice of coupling capacitors, due to the ability of handle large root-mean-square currents. The coupling capacitor C_{SEPIC} selection depends on the root-mean-square current. Due to a mismatch of a selected coupling capacitor C_{SEPIC} oscillation and in further consequence instability issues happens. In order to solve stability problems, a damping branch has to be placed in parallel to the coupling capacitor to increase controllability. In this way, lower ceramic capacitance value can be chosen and the damping branch can be build up by low cost electrolytic capacitors.

2.3.5 Utility Analysis DC/DC Converter

Outgoing from the findings of the presented bidirectional DC/DC voltage converter systems analysis is made. In Table 2.3 the comparison of the presented topologies through a utility analysis is shown on the next page.

2.3.6 Summary Converter System

The utility analysis from Subsection 2.3.5 has shown that the synchronous buck-boost converter is the choice of use for the further system design. The decision is based in particular on its positive aspects. On the one hand, through its H-Bridge implementation, it can be used in a wide variety of applications and thus brings with it a high degree of industrialization, while on the other hand high flexibility is guaranteed. The system allows for instance operations in buck, boost or buck-boost mode depending on the input to the output voltage. This capability leads to the positive effect of reducing switching losses, as the system can operate as a buck or boost converter during power flow control. In comparison to the Cuk and Sepic converter less passive components have to be used, whereas a higher efficiency in high power conversions will be achievable. The only disadvantage that can be noted is the control of the high-side switches.

Cuk and Sepic present alternative forms of bidirectional buck-boost converters. They gain positive aspects with their low ripple current at the input and output. However, these positive effects are not outweighed by the fact that almost two equally large storage inductances are required. Due to the expected high current ratings during the discharge phase, it is assumed that the electrical component arrangement will be very difficult to realize. Another major adverse effect is the number of passive components and their dissipation losses.

Table 2.3: Comparison of the presented bidirectional DC/DC converter

Converter Topologies	Amount of Components				Operation-Mode	Industri-alization	Peripherie	Voltage at the Switches	Total Points
	L	C	R	T					
Snychronuous buck-boost converter	1	2	0	4	10	9		6	35
Cuk converter	2	3 (4)	0 (1)	2	3	5	8	5	28
Sepic converter	2	3 (4)	0 (1)	2	4	5	5	6	27

2.3.7 Summary Concept Phase

In this chapter, the main effort was to get a thorough knowledge of energy storage types and DC-DC converter topologies. Outgoing from the requirements for both subsystems, a representation of the most common findings of the literature is presented. By using this investigation a utility analysis is made in order to find the particular system assembly to solve the stated problem. In this way, the aluminium electrolytic capacitor is selected as an energy storage unit. The main advantages are the high voltage ratings combined with the low effort of building up a capacitor bank. In addition, they are well suited for high ripple currents but due to their size and form-factor, they achieve very low energy density levels. The second key component is the power conversion converter. In an analogue way as with the energy storage system, the converter topology is chosen in accordance to fulfil the specified requirements, see Subsection 1.5.2. With the aid of the utility analysis, the synchronous buck-boost converter is the preferred choice for an extended system design. This decision is covered by the positive effects that the converter shines with high operation mode ability, less passive components and high efficiency in high power conversion applications. In the ongoing next Chapter 3 the complete system design process is conducted. In the first design stage, the energy storage unit will be defined and composed while in further steps an analytic calculation of the energy storage system process is made. Further the converter will be dimensioned and analysed based on static and dynamic analysis approaches.

3 System Design

In the previous Chapter 2, the concept phase was carried out. This chapter now deals with the system design. The first part of this chapter focus on the energy storage design in order to meet the requirements of storing energy levels up to $4.3\mathrm{kJ}$. In the second part of this chapter, analytical mathematical analysis of the stated problem during the discharge phase in combination with the designed energy storage unit is carried out. From this quite theoretical analysis, important information can be gathered about the energy storage system design. Together with the processed converter analysis and the aforementioned analytic representation of the charging process a target design and sizing of the converter can be carried out.

3.1 Energy Storage System Design

The conceptual design for the energy storage system in Section 2.1 depicts that the aluminium electrolytic capacitor variant is used. In the following Subsection 3.1.1 the storage capacitor is designed based on the maximum power performance specification of the VLF generator.

3.1.1 Calculation and Selection of the Energy Storage Capacitor

In general, it can be stated that the amount of energy that shall be stored in the energy storage capacitor depends mainly on the selected VLF generator test voltage $U_{vlf,peak}$ as well as the tested power cable capacitance C_{cable}. The maximum performance data which can be achieved by a VLF test system during the AC withstand test are shown in Table 3.1.

Table 3.1: Parameter list for calculation of the secondary capacitor, which depends on the technical boundary conditions and the defined charging voltage range of the capacitor

Technical boundary conditions VLF-System			Charging voltage range	
$f_{vlf}[\mathrm{Hz}]$	$U_{vlf,peak}[\mathrm{kV}]$	$C_{cable}[\mu\mathrm{F}]$	$U_{s,min}[\mathrm{V}]$	$U_{s,max}[\mathrm{V}]$
0.1	65	2	60	360

First, a relationship between the storage capacitor and the stored energy content must be found. With the help of the capacitor energy Formula 3.1 the amount of stored energy in a power cable can be calculated.

$$E = \frac{1}{2} \cdot C \cdot U^2 \tag{3.1}$$

The maximum energy level under maximum power settings in a a VLF system is

$$E_{vlf,peak} = \frac{1}{2} \cdot C_{cable} \cdot U^2_{vlf,peak}$$
$$\underline{E_{vlf,peak} = 4225\text{J}.}$$

The injected maximum energy $E_{vlf,peak}$ from the VLF generator into the power cable $C_{cable} = 2\mu\text{F}$ during the first quarter period of the very-low frequency voltage sine wave depends mainly on $U_{vlf,peak}$. This amount of energy is that one that has to be stored during the discharge phase of the power cable.

By applying the law of conservation of energy in order to store the discharge energy the following Equation 3.2 is defined.

$$\Delta E_s = \frac{1}{2} \cdot C_s \cdot \left(U^2_{s,max} - U^2_{s,min}\right) \tag{3.2}$$

The above stated equation results from the consideration of the requirements in Subsection 1.5.1 for the energy storage unit, where the discharged energy shall be stored between the voltage levels $U_{s,min}$ and $U_{s,max}$. The index s defines always the storage unit itself. Through modification and the insertion of the discharge energy $E_{vlf,peak}$ instead of ΔE_s leads to Equation 3.3.

$$C_s = \frac{2 \cdot E_{vlf,peak}}{U^2_{s,max} - U^2_{s,min}}. \tag{3.3}$$

By inserting the requirements and the maximum energy rating $E_{vlf,peak}$ the capacitor storage capacitance is dimensioned. The storage capacitance must have a minimum capacitance of

$$\underline{C_s = 71 \text{ mF}}.$$

In summary, it can be stated that the calculated storage capacitance depends mainly on the extracted discharge energy $E_{vlf,peak}$ from the power cable and on the voltage variability ($U_{s,min}$ to $U_{s,max}$). The minimum voltage value $U_{s,min}$ shall allow with regard to the power flow control a non-violation of the lower duty cycle value. For more information on duty cycle limits with respect to the power flow control, see Section 3.3, where the synchronous converter topology is sized to meet the interdependent requirements between the storage unit and the converter unit.

3.1.2 Selection and Sizing of Aluminium Electrolytic Capacitor Bank

In the ongoing design process, the underlying stated problem in Section 1.1, as well as the requirements for the energy storage system from Subsection 1.5.1, will always stay in focus of the dimensioning and its selection. Based on the maximum intermediate storage voltage $U_{s,max}$ and the determined capacitance C_s the sizing and selection are done.

Before the capacitor bank is dimensioned, aging effects due to capacitance losses and changes in the equivalent series resistor R_{ESR} are discussed. Only the most important findings about aging mechanisms are presented and shall be considered in the selection process. The life of a capacitor is mainly determined by the change in its characteristics over time. In the case, of the capacitor characteristics, this means a decrease in capacitance C and the increase of the internal resistance R_{ESR} occurs, as mentioned by Literature [13]. Aging is particularly dependent mostly on temperature. This is also the reason why the manufacturer specifies the lifetime in relation to a maximum temperature. On the basis from Literature [10] changes in capacitance of -5% and changes in R_{ESR} of $+20\%$ under DC-Voltage bias test conditions can be expected. Such effects must be taken into account in each application to guarantee lifetime and not end up in an early failure when defining an energy storage unit.

Through this statement, the energy storage capacitance is defined with a design factor S of 10 $\%$ for the capacitance C_s and for the nominal rated voltage U_{DC}. For the selection a total storage capacitance of $C_S \geq 78.1\mathrm{mF}$ and for the nominal voltage $U_{DC} \geq 385\mathrm{V}$ has to be achieved.

An appropriate choice of the storage capacitor is the ALS70/71 aluminium electrolytic capacitor series from KEMET. It offers tremendous performance in capacitance and nominal voltage ratings. Additionally it features high ripple currents and can perform over a long lifetime with a high efficiency, which is desired due to the requirements.

In Table 3.2 the characteristic parameters of the aluminium electrolytic capacitor of type ALS71H203QT400 are illustrated.

Table 3.2: Performance characteristic parameters of the selected aluminium electroclytic capacatior ALS71H203QT400

Symbol	Meaning	Type/ Value	Unit
-	Part Number	ALS71H203QT400	[ ]
U_{DC}	Nominal Voltage Rating	400	$[\mathrm{V}]$
C	Rated Capacitance	20	$[\mathrm{mF}]$
ΔI	Ripple Current	29.1	$[\mathrm{A}]$
$R_{ESR,C}$	Equivalent Series Resistance	12	$[\mathrm{m\Omega}]$

Outgoing from the selected storage capacitor in Table 3.2 the capacitor bank can be sized. With the use of the presented Equation 3.4 the equivalent total capacitance and

total equivalent series resistor can be calculated. Let $n = n_{s,cell,series}$ the number of cells in a series string connection and $m = n_{s,cell,parallel}$ the number of cells in parallel branches.

$$C_{Total} = C_{Cell} \cdot \frac{m}{n} \qquad R_{Total} = R_{Cell} \cdot \frac{n}{m} \tag{3.4}$$

Since the nominal voltage of a single capacitor cell exceeds the limit of $U_{DC} \geq 385\mathrm{V}$ the series number of cells can be defined by $n_{s,cell,series} = 1$.

The number of parallel capacitor cells $n_{s,cell,parallel}$, in order to achieve the desired capacitance C_s is defined by Equation 3.5. The ceil command rounds the number of determined parallel branches to the next higher integer number.

$$n_{s,cell,parallel} = ceil\left(\frac{C_s}{C} \cdot n_{s,cell,series}\right) \tag{3.5}$$

According to the specification list in Table 1.2 the nominal rated voltage of $\geq 350\mathrm{V}$ is achieved with the capacitor from Table 3.1.

The total number of parallel cells counts

$$n_{s,cell,parallel} = 4$$

.

A recalculation of the overall equivalent capacitor C_s by inserting the number of cells in parallel and series connection into Equation 3.4 leads to a final total capacitance of

$$\underline{\underline{C_s = 80\ \mathrm{mF.}}}$$

For further use especially when modelling the storage capacitor the overall equivalent series resistance is calculated. Due to this the dissipation losses in the simulation can be displayed. Additionally, the capacitors time response of the capacitor bank can be calculated ($\tau_C = R_{ESR,C} \cdot C$). Equation 3.6 derives the total equivalent series resistor for the sized energy storage capacitor bank.

$$R_{ESR,C_s} = \frac{n_{s,cell,series}}{n_{s,cell,parallel}} \cdot R_{ESR,C} \tag{3.6}$$

The total given equivalent series resistor is $R_{ESR,C_s} = 3\mathrm{m}\Omega$. Transition resistances are excluded in the current design process. Finally, the following Subsection 3.1.3 compares the dimensioned aluminium electrolytic storage capacitor bank with an equal super-capacitor bank.

3.1.3 Comparison Aluminium Electrolytic Capacitor Bank with Supercapacitor Bank

Despite the fact of choosing the aluminium electrolytic capacitor for the final system design, a comparison between supercapacitor and ALC has nevertheless been made, due to their close result in the conducted utility analysis in Section 2.2. The energy storage design and sizing is made in an analogous way to the aluminium electrolytic capacitor variant with the supercapacitor variant. Table 3.3 presents the final result. It is remarkable that building up a supercapacitor module takes much greater effort as compared to ALC. This fact is due to the lower cell voltage U_{cell}. The gravimetric energy density on the one hand for supercapacitors is greater due to their lower total mass while on the other hand, the final response time of ALC are faster by a factor of six. The choice of the supercapacitor was made in such a way that only one serial string of the capacitor bank must be executed. This saves additional circuitry effort since no parallel branches have to be made.

Table 3.3: Comparison between aluminium electrolytic capacitor module and supercapacitor module

Storage Type	Rated Cell Capacitance C [F]	Rated Cell Voltage U_{cell} [V]	Cpacitor Module		Total Mass m_{total} [kg]	Capacitor Module Response Time τ [ms]	Energy Density E_{GRAV} [Wh/s]
Aluminium Electrolytic Capacitor Manufacturer: *"Kemet" "ALS71H203QT400"*	0.02	400	4 (parallel)	1 (series)	8	0.24	0.21
Super-Capacitor Manufacturer: *"Vishay" "MAL223091009E3"*	10	3	1 (parallel)	129 (series)	3.24	1.4	1.61

3.1.4 Summary of Calculation and Selection of the Energy Storage Capacitor

In this section, the main focus was set on the storage capacitor design to absorb the provided discharge energy. In accordance with the design procedure, it is basically aimed that the nominal voltage U_{DC} of the capacitor bank is larger than the maximum charging voltage $U_{s,max}$. This also minimizes the risk of over-voltages by a percentage factor. With utmost certainty, safety circuitry using surge arresters must also be taken into account in the system design for later use. The overall setup for the energy storage unit consists of an energy storage device that has four capacitor cells of type ALS71H203QT400 in parallel with a total capacitance of $C_s = 80\mathrm{mF}$ and an total equivalent resistor $R_{ESR,C_s} = 3\mathrm{m}\Omega$. The single cell capacitance response time is $\tau_{C,single,cell} = 0.24\mathrm{ms}$.

Through the selected power converter between the high voltage DC bus side (primary side) and low voltage DC bus side (secondary side) of the capacitor bank a controlled power flow transfer has to be managed. In the next Section 3.2 the linkage between the stated problem and the use of the designed energy storage capacitor is done to derive an analytic solution to the energy storage process.

3.2 Analytical Calculation of the Energy Charging Process

In this section, an analytical calculation of the energy recovery process during the discharge phase in a VLF test environment is performed. The designed intermediate storage capacitor bank from Section 3.1 will be used to store the discharge energy $E_{cable}(t)$ of the cable. In advance, the analytical calculation provides information about the charging current $i_s(t)$ and the temporal change of the charging voltage $u_s(t)$ during the discharge phase ($t_{dis} = 0\text{s}$ to $t_{dis} = 2.5\text{s}$). Based on the stated problem in Subsection 1.1 and the use of the dimensioned electrical energy storage unit from Section 3.1 the following parameters are known, see Table 3.4.

Table 3.4: Parameter list for the analytical calculation of the energy charging process

Symbol	Meaning	Type/ Value	Unit
f_{vlf}	Very-low frequency	0.1	[Hz]
$U_{vlf,peak}$	Peak voltage VLF generator	65	[kV]
C_{cable}	Power cable capacitance	2	[µF]
C_s	Energy storage capacitor	0.08	[F]
$U_{s,min}$	Minimum charge voltage	60	[V]
$U_{s,max}$	Maximum charge voltage	350	[V]
t_{dis}	Discharge time	2.5	[s]

It has to be remarked that the analytical calculation is carried out for the maximum performance data of the VLF system. The performance data are extracted out of a product called Viola from the company Baur GmbH. This device represents a VLF test and diagnostic device that can be used to evaluate the condition of insulated high voltage cables.

The complete calculation is done under ideal conditions. The power cable is modeled as an ideal capacitor, where no leakage current is expected. In the reverse power flow direction, the discharge energy is transferred from the high voltage cable side to the energy storage unit. The VLF test voltage $u_{vlf}(t) = u_{cable}(t)$ can modeled analytically with Equation 3.7.

$$u_{vlf}(t) = U_{vlf,peak} \cdot \sin(2 \cdot \pi \cdot f_{vlf} \cdot t) \tag{3.7}$$

The resulting current over time in the power cable is calculated via the differential equation of the capacitor, see Equation 3.8. The power cable is assumed to be ideal and can be therefore represented as a single capacitor.

$$i_{cable}(t) = C_{cable} \cdot \frac{\mathrm{d}u_{cable}}{\mathrm{d}t} = C_{cable} \cdot U_{vlf,peak} \cdot \cos(2 \cdot \pi \cdot f_{vlf} \cdot t). \tag{3.8}$$

Through Equation 3.7 and 3.8 the power over time $p_{cable}(t)$ is calculated. Let ω_0 be representative for $2 \cdot \pi \cdot f_{vlf}$.

$$p_{cable}(t) = \frac{U_{vlf,peak}^2 \cdot C_{cable} \cdot \omega_0}{2} \cdot \sin\left(2 \cdot \omega_0 \cdot t\right) \tag{3.9}$$

Figure 3.1 illustrates the power over time $p_{cable}(t)$ for the maximum performance of the VLF generator. It can be noted that a peak power $P_{cable,peak}$ of $\approx 2.7\mathrm{kW}$ is active during the total discharging phase t_{dis}.

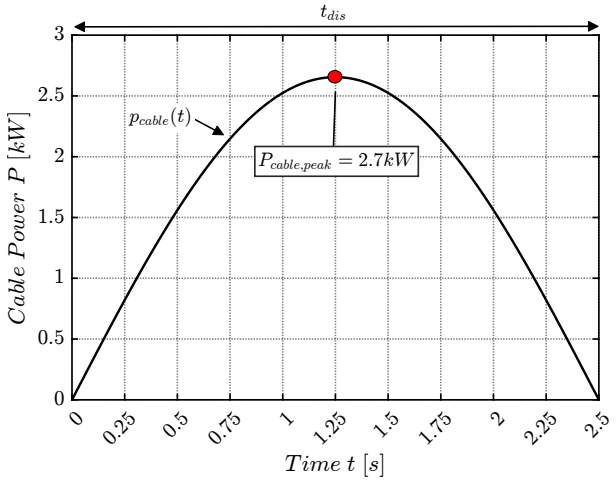

Figure 3.1: Power curve during discharge phase of the high-voltage power cable

From the temporal power flow $p_{cable}(t)$, the temporal change of the discharge energy can now be calculated through an integration over the complete discharge phase $t_{dis} = 2.5\mathrm{s}$. Equation 3.10 presents the energy over time in the reverse power mode.

$$E_{cable}(t) = \frac{U_{vlf,peak}^2 \cdot C_{cable} \cdot \omega_0}{2} \int_0^{t_{dis}} sin(2 \cdot \omega_0 \cdot t)\ dt \tag{3.10}$$

$$E_{cable}(t) = \frac{U_{vlf,peak}^2 \cdot C_{cable}}{4} \cdot \left(1 - \cos\left(\frac{4 \cdot \pi}{T_{vlf}} \cdot t\right)\right)$$

The energy over time which is extracted behaves as a $1 - cos()$ function and is represented in Figure 3.2.

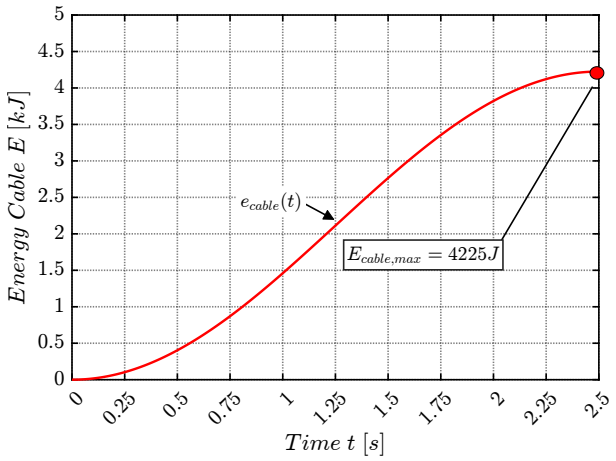

Figure 3.2: Discharge energy over time of the high-voltage power cable

The input voltage waveform at the discharge circuit input is shown in Figure 3.3. Based on a new development of the VLF system by Baur GmbH a bidirectional power flow is enabled. This causes a transformation of the underlying test voltage $u_{vlf}(t)$ (peak voltage of $65\mathrm{kV}$) up to $1.1\mathrm{kV}$ at the input side of the discharge circuit.

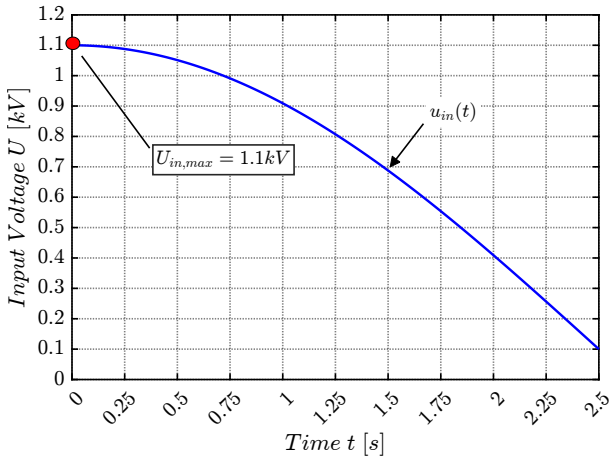

Figure 3.3: Input voltage curve over time at the discharge circuit

The mathematical model of the input voltage at the discharge circuit is given by equation

$$u_{in}(t) = 1100 \cdot \sin(2 \cdot \pi \cdot f_{vlf} \cdot t). \tag{3.11}$$

The law of conservation of energy links the analytic calculation to the designed aluminium electrolytic bank. The energy balance analysis permits to add of the energy components of the discharge energy $E_{cable}(t)$ and the initial energy at the energy storage unit $E_{s,initial}$. The resulting amount of energy is shown in Equation 3.12. $E_{s,initial}$ describes the initial steady-state energy of the energy storage unit at time $t_{dis} = 0\mathrm{s}$.

$$E_s = E_{s,initial} + E_{cable}(t) \tag{3.12}$$

Through subsequently inserting the already existing Equations 3.10 in Equation 3.12 leads to Equation

$$\frac{C_s \cdot U_s^2}{2} = \frac{C_s \cdot U_{s,min}^2}{2} + \frac{U_{vlf,peak}^2 \cdot C_{cable}}{4} \cdot \left(1 - \cos\left(\frac{4 \cdot \pi}{T_{vlf}} \cdot t\right)\right). \tag{3.13}$$

By modifying Equation 3.13, the storage voltage over time $u_s(t)$ is derived, see Equation 3.14.

$$u_s(t) = \sqrt{U_{s,min}^2 + \frac{U_{vlf,peak}^2 \cdot C_{cable}}{2 \cdot C_s} \cdot \left(1 - \cos\left(\frac{4 \cdot \pi}{T_{vlf}} \cdot t\right)\right)} \tag{3.14}$$

In Figure 3.4 the charging voltage $u_s(t)$ is illustrated. It can be noted that the requirements from Subsection 1.5.1 with regard to the minimum and maximum charging voltage levels are met.

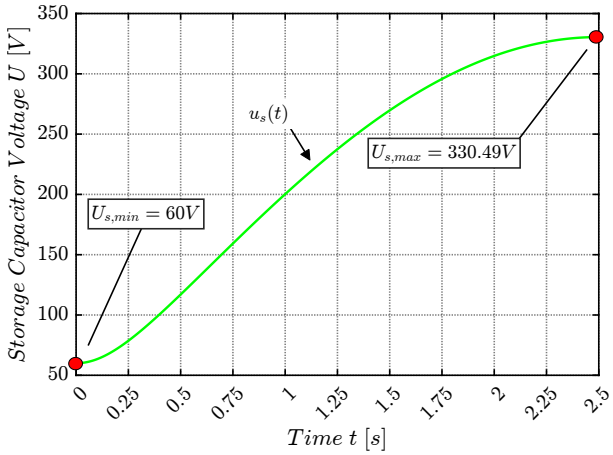

Figure 3.4: Analytic solution for the charging voltage over time $u_s(t)$at the aluminium electrolytic storage capacitor C_s

To derive the charging current over time $i_s(t)$ the derivative of the charging voltage equation $u_s(t)$ has to be conducted. The derivative represents the rate of change of the storage capacitor voltage $u_s(t)$ during charging. By applying the differential equation of a capacitor allows us to describe the charging process of the storage capacitor with regard to its charging current. In Equation 3.15 the solution for the charging current $i_s(t)$ is presented.

$$i_{s(t)} = \frac{U_{vlf,peak}^2 \cdot C_{cable} \cdot \pi \cdot \sin\left(\frac{4 \cdot \pi}{T_{vlf}} \cdot t\right)}{T_{vlf} \cdot \sqrt{\frac{U_{s,min}^2 \cdot 2 \cdot C_s + U_{vlf,peak}^2 \cdot C_{cable} \cdot \left(1 - \cos\left(\frac{4 \cdot \pi}{T_{vlf}} \cdot t\right)\right)}{2 \cdot C_s}}} \tag{3.15}$$

Figure 3.5 shows the graphical representation of $i_s(t)$. The maximum peak charging current $I_{s,max}$ is 13.59A.

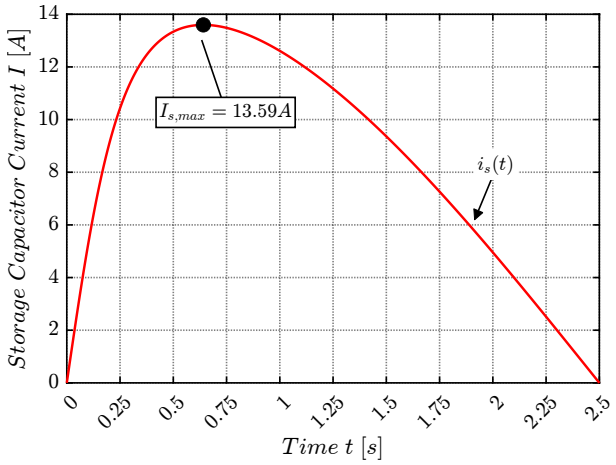

Figure 3.5: Analytic solution for the charging current over time $i_s(t)$ at the aluminium electrolytic storage capacitor C_s

3.2.1 Summary Analytical Calculation

By using the analytical calculation which is described above, it was possible to derive other time-based quantities such as the discharge energy $E_{cable}(t)$, the charge voltage $u_s(t)$ and the charge current $i_s(t)$ at the aluminium electrolytic storage capacitor. The analytical solution is verified by applying a cross-check. The product of the charging current $i_s(t)$ and the charging voltage $u_s(t)$ must correspond to the power flow $p_{cable}(t)$ during the discharge phase of the power cable. Figure 3.6 shows that both power curves are congruent.

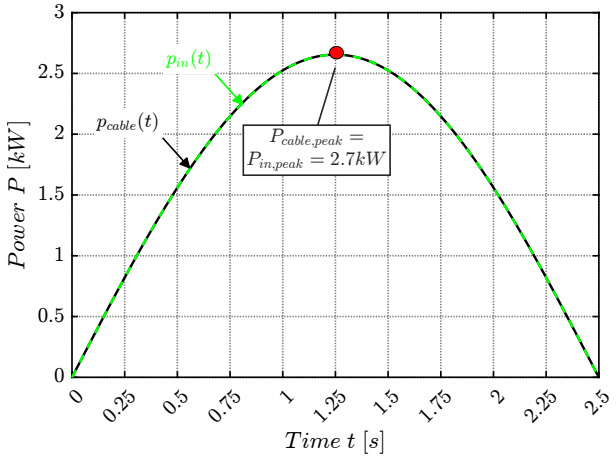

Figure 3.6: Proof of Power-Flow $P_{(t)}$

It can be noted, that the analytical calculation is successful. In the next section 3.3, the synchronous buck-boost converter is described in a more detailed way in its working

principle. By taking into account the converter functionality and the elaboration of the analytical solution from Section 3.2 , a dimensioning design of the synchronous buck-boost converter is presented.

3.3 Synchronous Buck-Boost Converter

The main objective in this section is the dimensioning of the synchronous buck-boost converter to meet the converter requirements from Subsection 1.5.2. In order to do this, first a thorough understanding of the circuitry is necessary. Only from this point of view, it is possible to establish a connection between the analytical calculation from Section 3.2 and the converter topology.

In the ongoing Subsection 3.3.2 it will be clarified in which operating mode the buck-boost converter is driven during the energy recovery process. Afterwards, the basic operation of the synchronous buck-boost converter for the selected operation mode in Subsection 3.3.2 is presented. Outgoing from the gathered functional principle the steady state analysis is conducted. Furthermore, an AC modeling approach is performed by applying the state-space-averaging modeling technique in Subsection 3.3.8 to perform in later stages the closed-loop controller design. The calculation rules for determining the inductance value, as well as the calculation of the time current characteristics in the individual components, are also part of this section too.

3.3.1 Selection of the Operating Principle

The synchronized buck-boost converter allows high flexibility in selecting operating modes. Depending on the primary input voltage $u_{in}(t)$ compared to the secondary output voltage $u_s(t)$ the converter is able to operate in synchronize buck, synchronize boost or synchronize buck-boost mode. The first two modes have the advantage that only two switches in the H-Bridge are switching, in which the switching losses can be reduced to half. But for the current design process the synchronized buck-boost mode is selected. The reason is that this mode enables a higher transformation ratios between inductor current versus load current [29]. This will be prove to be an advantage in the desired application, due to the high power flow ratings. Another background of this selection is that no additional mode selection circuit for the ongoing design process must be implemented. This reduces the system complexity and allows much easier control of the converter. The only disadvantage is that higher switching losses will occur. Further information about the operating principles, the mode selection circuit and the use case of the three modes in a specific application can be found in Literature [29]. In summary, this subsection has presented the choice of the converter operating principle which is used for further investigations and analysis.

3.3.2 Functional Converter Principle

The general principle of the synchronous buck-boost converter in its buck-boost operating mode is presented. In Figure 3.7 the chosen topology scheme is schematically presented.

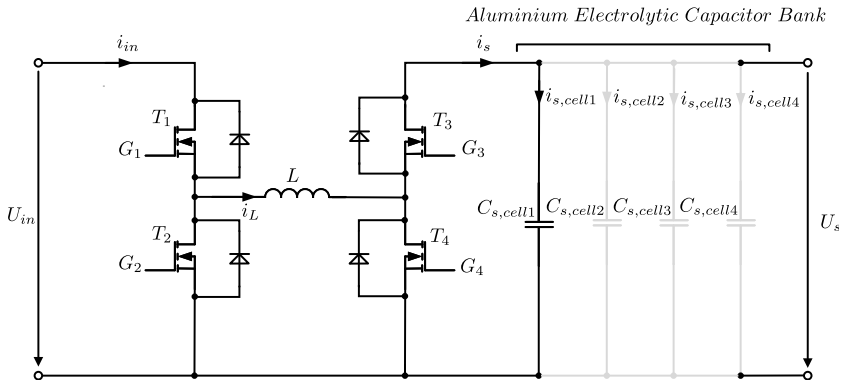

Figure 3.7: Topology scheme of a synchronous buck-boost converter which charges the secondary output capacitance via the storage inductor in the middle H-Bridge cross path

Based on the selected buck-boost operating mode the following switching state table is given:

Table 3.5: Switching states for MOSFET T_1, T_2, T_3 and T_4 in buck-boost operation mode

Operating Mode	T_1	T_2	T_3	T_4
buck-boost	D	$1-D$	$1-D$	D

Table 3.5 defines the gate signals G_1, G_2, G_3 and G_4 with accordance to the duty cycle D for the power MOSFET switches T_1, T_2, T_3 and T_4.

In Table 3.6 the mathematical representation of the inductor over time signal trace are shown.

Table 3.6: Definition of the inductor over time signal trace

Phase	Interval	Signal trace
$D \cdot T_{sw}$	$0 \leq t \leq D \cdot T_{sw}$	$I_{L,min} + \frac{U_{in} \cdot D \cdot T_{sw}}{L}$
$(1-D) \cdot T_{sw}$	$0 \geq t \geq (1-D) \cdot T_{sw}$	$I_{L,max} - \frac{U_{out} \cdot (1-D) \cdot T_{sw}}{L}$

In Figure 3.8 the gate control signals are schematically shown.

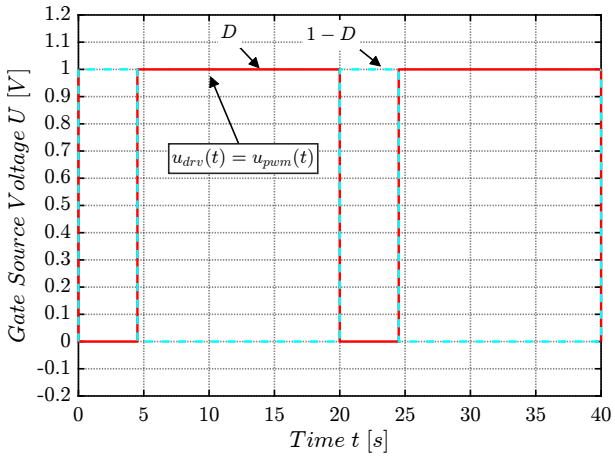

Figure 3.8: Control signals of the MOSFET T_1, T_2, T_3 and T_4 for the buck-boost operating mode

Due to the switching states, the following input current $i_{in}(t)$ and the inductor current $i_L(t)$ results, see Figure 3.9.

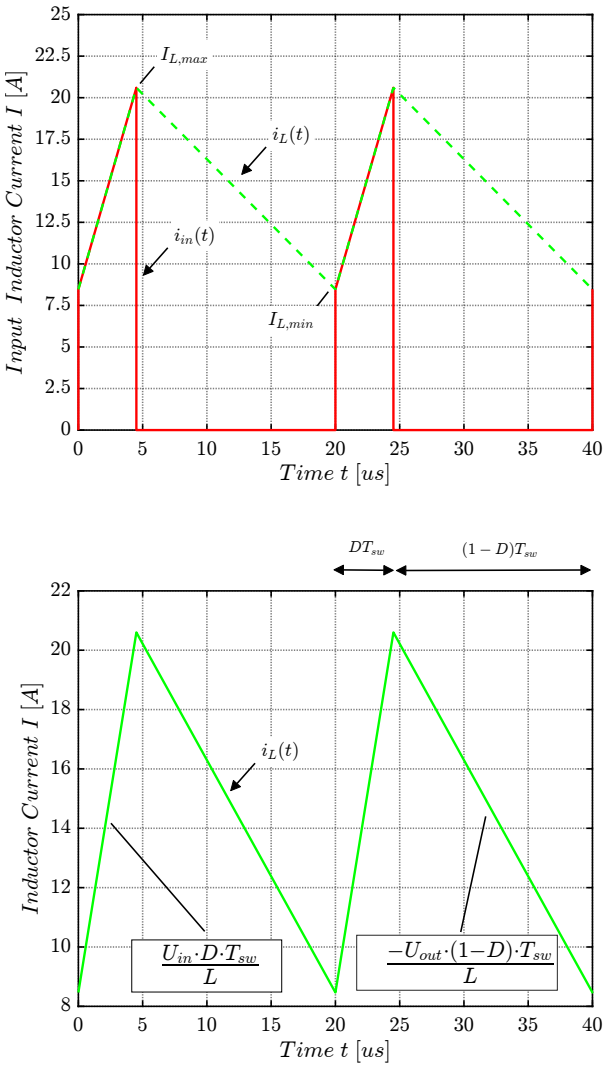

Figure 3.9: Exemplary illustrative representation of the inductor current i_L and the input current i_{in} of a synchronous buck-boost converter in buck-boost operation mode

The findings from the functional operating principle are the basis for the ongoing steady state analysis in Subsection 3.3.3. This analysis provides system related functional correlations for enabling the required continuous conduction mode.

3.3.3 Steady State Analysis

According to the requirements from Subsection 1.5.1 the synchronous buck-boost shall be dimensioned to work in continuous conduction mode. Capital letters in the analysis represent static or averaged quantities. The steady state analysis is conducted with ideal components and delivers important informations about mean inductor current value I_L and mean output voltage $U_s = U_{out} = U_R = U_C$.

The steady state analysis is proceeded in the following way:

- Analysis of Subcircuit: $D \cdot T_{sw} = t_{on}$
- Analysis of Subcircuit: $(1 - D) \cdot T_{sw} = t_{off}$
- Applying Volt-Second-Balance and Ampere-Second-Balance over one switching cycle T_{sw}

3.3.3.1 Analysis Subcircuit: $D \cdot T_{sw}$:

In Figure 3.10 the sub-circuit for switching phase $D \cdot T_{sw}$ is shown. In this phase the inductor is charged.

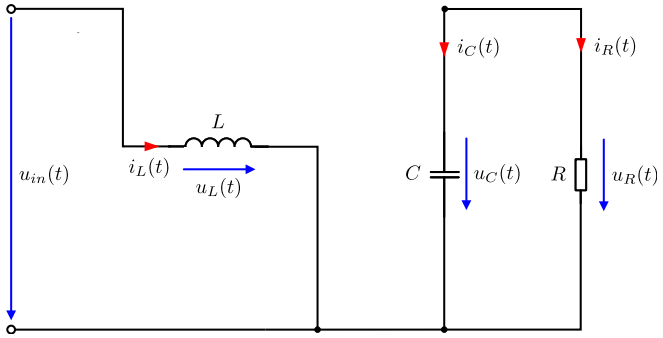

Figure 3.10: Subcircuit for switching position $D \cdot Tsw$

With the use of Kirchhoff's law the inductor voltage $u_L(t)^{ton}$ and capacitor current $i_C(t)^{ton}$ during the charging phase are derived.

$$u_L(t)^{ton} = u_{in}(t) \tag{3.16}$$

$$i_c(t)^{ton} = -i_R(t) = \frac{-u_{out}(t)}{R} \tag{3.17}$$

Equations 3.18 and 3.19 represent the averaged quantities of inductor voltage and capacitor current when applying the small ripple approximation.

$$U_L^{ton} = U_{in} \tag{3.18}$$

$$I_C^{ton} = \frac{-U_{out}}{R} \tag{3.19}$$

3.3.3.2 Analysis Sub-circuit: $(1 - D) \cdot T_{sw}$:

The second sub-circuit in Figure 3.11 shows the discharge phase of the inductor.

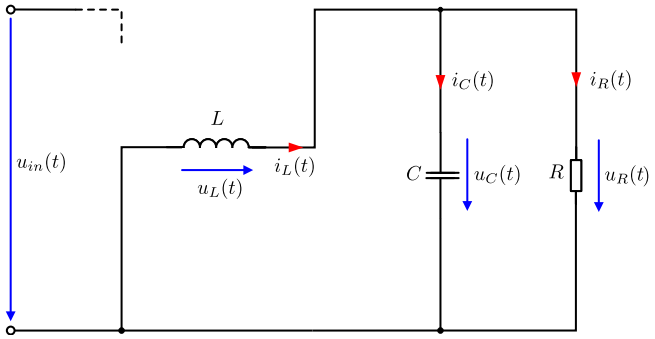

Figure 3.11: Sub-circuit for switching position $(1 - D) \cdot Tsw$

In analogous way the inductor voltage $u_L(t)^{toff}$ and capacitor current $i_C(t)^{toff}$ is derived.

$$u_L(t)^{toff} = -u_{out}(t) \tag{3.20}$$

$$i_C(t)^{toff} = i_L(t) - \frac{u_{out}(t)}{R} \tag{3.21}$$

The small ripple approximation leads then to the following Equations 3.22 and 3.23.

$$U_L^{toff} = -U_{out} \tag{3.22}$$

$$I_C^{toff} = I_L - \frac{U_{out}}{R} \tag{3.23}$$

Volt-Second Balance

Through applying the Volt-Second-Balance over one switching cycle T_{sw} a relation between output voltage $U_{out} = U_R$, duty cycle D and input voltage U_{in} is generated.

$$< U_L >= \frac{1}{T_{sw}} \cdot \int_0^{T_{sw}} v_{L(t)}\, dt = 0 \tag{3.24}$$

The characteristic voltage conversion equation between the input voltage and the output voltage is given by

$$U_{out} = \frac{D}{1-D} \cdot U_{in}. \tag{3.25}$$

Ampere-Second Balance

Through applying the Ampere-Second-Balance over one switching cycle, see Equation 3.26 Equation 3.27 is derived. In this equation the averaged mean inductor current I_L is presented.

$$< I_C >= \frac{1}{T_{sw}} \cdot \int_0^{T_{sw}} i_{C(t)}\, dt = 0 \tag{3.26}$$

$$I_L = \frac{U_{out}}{R} \cdot \frac{1}{1-D} \tag{3.27}$$

Output Voltage Ripple:

This kind of observation through the steady state analysis is not necessary. The output capacitor has been still dimensioned. Information about the dimensioned energy storage capacitor can be viewed in Section 3.1.

Ripple Choke Current:

The ripple inductor current for dimensioning the inductor L can be then given by Equation 3.28.

$$L = \frac{U_{in} \cdot D \cdot T_{sw}}{2 \cdot \Delta i_L} \tag{3.28}$$

The inductor value L depends on the input voltage U_{in}, the duty cycle D, the switching period T_{sw} and the inductor ripple current Δi_L. A smaller inductor ripple current leads to a bigger inductance.

On the basis of the steady state analysis and the performed analytic calculation of the charging process in Section 3.2, it is now possible to obtain further average converter quantities with respect to the complete power flow control.

3.3.4 Analytic Duty Cycle over Time of Synchronous Buck-Boost Converter

The first quantity which can be extracted by combining steady state analysis and analytic calculation is the duty cycle D. Through the use of the characteristic voltage conversion equation 3.25 from the steady state analysis and the use of the charging voltage Equation 3.14 as well as the input voltage Equation 3.11 the duty cycle over time of the synchronous buck-boost converter can be calculated.

The duty at a specific operating point is calculated with equation

$$D = \frac{U_{out}}{U_{out} + U_{in}}. \tag{3.29}$$

By now inserting the aforementioned charging voltage equation

$$u_s(t) = \sqrt{U_{s,min}^2 + \frac{U_{vlf,peak}^2 \cdot C_{cable}}{2 \cdot C_s} \cdot \left(1 - \cos\left(\frac{4 \cdot \pi}{T_{vlf}} \cdot t\right)\right)}$$

and the input voltage equation

$$u_{in}(t) = 1100 \cdot \sin(2 \cdot \pi \cdot f_{vlf} \cdot t),$$

the duty cycle over time $d(t)$ is calculated. In Figure 3.12 the duty cycle over time signal is displayed.

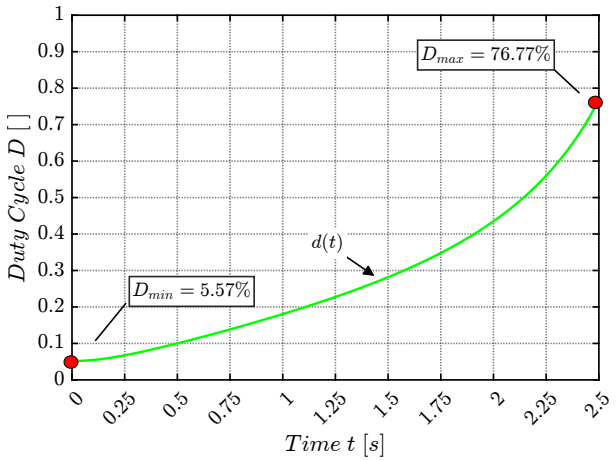

Figure 3.12: Analytic solution converter duty-cycle over time $d(t)$

It can be seen that in Figure 3.12 D_{min} and D_{max} do not violate the lower five percent and higher 95 percent of the duty cycle range. This leads to the result that the required duty cycle range is maintained.

3.3.5 Analytic Inductor Current over Time of Synchronous Buck-Boost Converter

The second quantity which can be extracted out of the combination between steady state analysis and analytic calculation is the averaged mean inductor current I_L.

Through Equation 3.27,

$$I_L = \frac{U_{out}}{R} \cdot \frac{1}{1-D}$$

the averaged inductor current under steady state condition is defined. During the complete charging process the output load is infinity. The output current ($\frac{U_{out}}{R}$) can be then replaced by the charging current $i_s(t)$ Equation 3.15.

$$i_{s(t)} = \frac{U_{vlf,peak}^2 \cdot C_c \cdot \pi \cdot \sin\left(\frac{4 \cdot \pi}{T_{vlf}} \cdot t\right)}{T_{vlf} \cdot \sqrt{\frac{U_{min}^2 \cdot 2 \cdot C_s + U_{vlf,peak}^2 \cdot C_{cable} \cdot \left(1 - \cos\left(\frac{4 \cdot \pi}{T_{vlf}} \cdot t\right)\right)}{2 \cdot C_s}}}$$

The obtained result of the averaged mean inductor current $i_L(t)$ during the energy recovery process is displayed in Figure 3.13 through the insertion of $d(t)$ and $i_s(t)$.

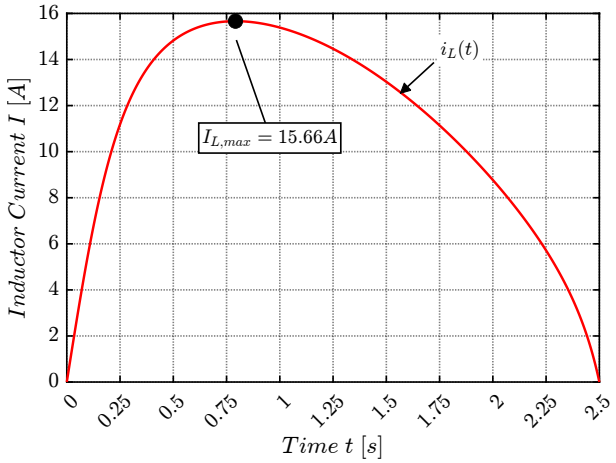

Figure 3.13: Analytic solution converter inductor current over time $i_L(t)$

A cross-check with the converters specification from Subsection 1.5.2 shows that the averaged inductor current range is specified. The maximum averaged inductor current is $I_{L,max} = 15.66\text{A}$.

3.3.6 Analytic Input Current over Time of Synchronous Buck-Boost Converter

The last unknown time-based quantity which can be determined is the input converter current $i_{in}(t)$. In the same way as for the derived duty cycle over time and the averaged inductor current, the input current of the synchronous buck-boost converter is calculated.

From Subsection 3.3.2 it can be identified that the input converter current is only active in the switching phase D. This permits to apply the following mathematical model for the input converter current, see Equation 3.30.

$$i_{in}(t) = i_L(t) \cdot d(t) \tag{3.30}$$

Also this equation is an averaged one. In Figure 3.14 the input current over time is illustrated over the complete charging period of 2.5s.

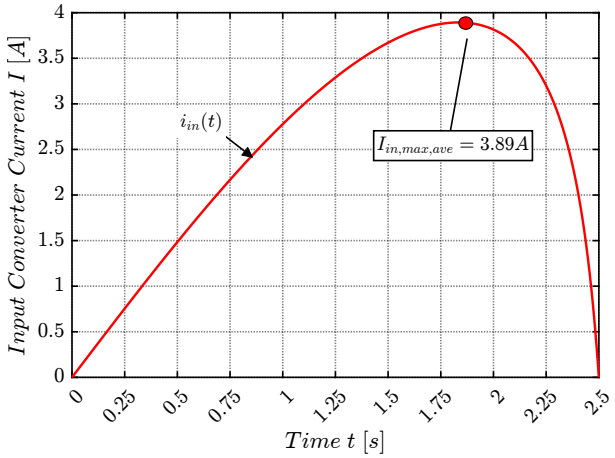

Figure 3.14: Analytic solution input converter current over time $i_{in}(t)$

3.3.7 Summary Theoretical Charging Process

With the use of the analytic calculation from Subsection 3.2 together with the steady state analysis from Section 3.3 further interdependent system quantities could be derived. At the present design process, all necessary averaged quantities are known to build up the complete charging process. The extracted theoretical time quantities with respect to the analytical charging process are shown up in Table 3.7.

Table 3.7: Analytical voltage and current time quantities which are extracted out of an theoretical analysis

Symbol	Meaning	Figure Number:
$i_{in}(t)$	Analytic averaged input convert current over time	3.14
$i_L(t)$	Analytic averaged inductor current over time	3.13
$d(t)$	Analytic duty cycle over time	3.12
$i_s(t)$	Analytic charging current over time	3.5
$u_s(t)$	Analytic charging voltage over time	3.4

Due to the theoretical power flow calculation, an analytic solution of the duty cycle $d(t)$ for controlling the energy storage system is given. This finally leads to the result that controlling the buck-boost converter with the analytic duty cycle $d(t)$ permits the energy transfer $E_{cable}(t)$ to the aluminium electrolytic capacitor bank in a correct manner.

3.3.8 State-Space-Averaging-Modeling

To set the next step toward controller design a more system-oriented investigation of the power converter is necessary. In this subsection, the main effort is taken to build up an AC model of the converter by using the state-space-averaging modeling technique [12]. During the switching of power MOSFETs non-linear current characteristics result. Reference [30] has observed that the switching components are the reason for non-linearity. The duty cycle $d(t)$ and the input voltage $u_{in}(t)$ represents the input quantities. Disturbance quantities will be not considered during state-space-averaging. In Figure 3.15 the buck-boost with its parasitic components is shown. The small signal model which shall be derived should include parasitic components.

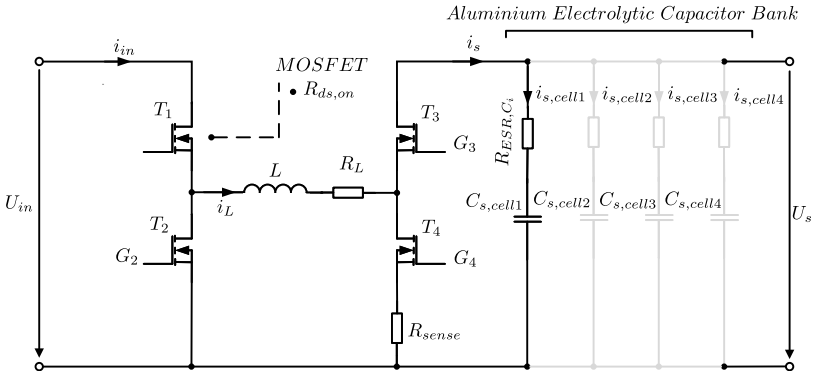

Figure 3.15: Schematic circuit of the synchronous buck-boost converter with parasitic

In Figure 3.25 a schematic representation of an operating OP_i and its meaning when deriving the small signal model is shown. It is illustrated that a change in the duty cycle causes a change in the input current. Due to the linearization, only a small perturbation $\tilde{d(t)}$ is possible, otherwise, deviations to the analog circuit system occur.

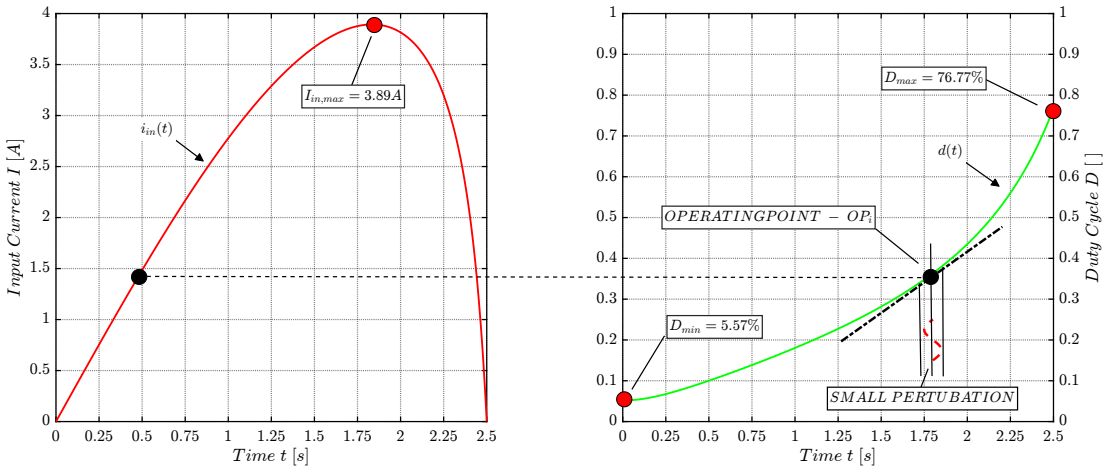

Figure 3.16: Operating point description for AC model analysis

In order to derive the dynamical small signal model of the the DC/DC converter an analysis of the linear circuit in Figure 3.15 must be made.

3.3.8.1 Analysis Subcircuit: $D \cdot Tsw$:

When MOSFET T_1 and T_4 are in on state the following subcircuit in Figure 3.17 is derived.

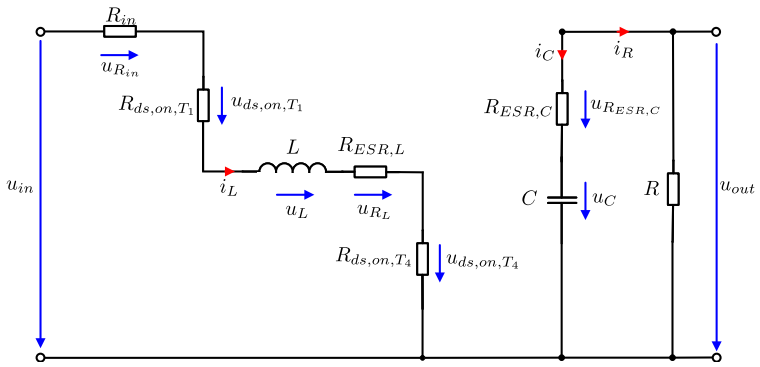

Figure 3.17: Buck-boost subcircuit $D \cdot T_{sw}$ for state-state-space-averaging modeling

Through the Kirchhoff's law the dynamical equations of inductor and capacitor for switching phase $D \cdot T_{sw}$ are derived and can be written as:

$$L \cdot \frac{\mathrm{d}i_L}{\mathrm{d}t} = u_{in} - (R_{in} + 2 \cdot R_{ds,on} + R_{ESR,L}) \cdot i_L \tag{3.31}$$

$$C \cdot \frac{\mathrm{d}u_C}{\mathrm{d}t} = -\frac{1}{R + R_{ESR,C}} \cdot u_C \tag{3.32}$$

The equation for the output load voltage as well as the input converter current can be written as:

$$u_{out} = \frac{R}{R + R_{ESR,C}} \cdot u_C \tag{3.33}$$

$$i_{in} = d \cdot i_L \tag{3.34}$$

3.3.8.2 Analysis Subcircuit: $(1-D)\cdot Tsw$:

When MOSFET T_2 and T_3 are in on state the following subcircuit in Figure 3.17 is derived.

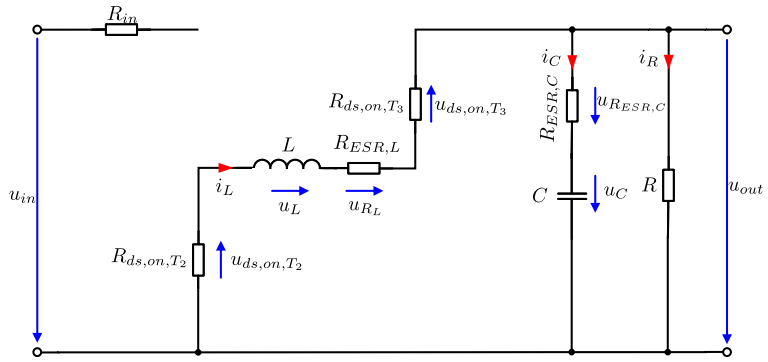

Figure 3.18: Buck-boost subcircuit $(1-D)\cdot T_{sw}$ for state-state-space-averaging modeling

In analogous way as before the dynamical equations for the inductor and capacitor are derived and can be written as:

$$L\cdot\frac{\mathrm{d}i_L}{\mathrm{d}t}=-\left(2\cdot R_{ds,on}+R_{ESR,L}+\frac{R_{ESR,C\cdot R}}{R+R_{ESR,C}}\right)\cdot i_L-\frac{R}{R+R_{ESR,C}}\cdot u_C \tag{3.35}$$

$$C\cdot\frac{\mathrm{d}u_C}{\mathrm{d}t}=-\frac{u_C}{R+R_{ESR,C}}+\frac{R}{R+R_{ESR,C}}\cdot i_L \tag{3.36}$$

$$u_{out}=\frac{R}{R+R_{ESR,C}}\cdot u_C+\frac{R_{ESR,C}\cdot R}{R+R_{ESR,C}}\cdot i_L \tag{3.37}$$

$$i_{in}=0 \tag{3.38}$$

3.3.8.3 Averaging of System Equations

After the general Equations from 3.31 to 3.37 are derived the averaging process is conducted. The basic equations for inductor voltage $u_L(t)$, capacitor current $i_C(t)$, output voltage $u_{out}(t)$ as well as the input current $i_{in}(t)$ are extended with the active duty cycle d which is present in this switching phase and the switching period T. The second switching phase is considered in the same way and extended by the expansion with $(1-D)$ and T_{sw}. The equations are then superimposed. The averaging is realized by multiplying both sides with $\frac{1}{T_{sw}}$.

This leads to the averaged differential equations for the inductor current 3.39 with its low-frequency averaged values.

$$L \cdot \frac{\mathrm{d}i_L}{\mathrm{d}t} = u_{in} \cdot d + R_1 \cdot i_L \cdot d + R_2 \cdot i_L \cdot (d-1) + R_3 \cdot u_C \cdot (d-1) \tag{3.39}$$

R_1, R_2 and R_3 represent following substitutions:

$$R_1 = -R_{in} - 2 \cdot R_{ds,on} - R_{ESR,L}$$

$$R_2 = 2 \cdot R_{ds,on} + R_{ESR,L} - \frac{R_{ESR,C \cdot R}}{R + R_{ESR,C}}$$

$$R_3 = \frac{R}{R + R_{ESR,C}}$$

The averaged differential equation for the capacitor current with its low-frequency averaged values is shown in Equation 3.40 .

$$C \cdot \frac{\mathrm{d}u_C}{\mathrm{d}t} = R_4 \cdot u_C \cdot d + R_5 \cdot u_C \cdot (d-1) + R_6 \cdot i_L \cdot (1-d) \tag{3.40}$$

R_4, R_5 and R_6 represent following substitutions:

$$R_4 = -\frac{1}{R + R_{ESR,C}}$$

$$R_5 = \frac{1}{R + R_{ESR,C}}$$

$$R_6 = \frac{R}{R + R_{ESR,C}}$$

The averaged output equation with its low frequency averaged values is shown in3.41.

$$u_{out} = R_6 \cdot u_C + R_7 \cdot i_L \cdot (1-d) \tag{3.41}$$

R_7 represent following substitution:

$$R_7 = \frac{R_{ESR,C} \cdot R}{R_{ESR,C} + R}$$

The averaged input current equation with its low frequency averaged values is shown in Equation 3.42.

$$i_{in} = d \cdot i_L \tag{3.42}$$

3.3.8.4 Linearization of the Averaged System Equations around the Operating Point

After the averaged system is derived the equations are linearized around the operating point using differentiation. A graphical representation can be seen in Figure 3.16.

The linearization is done by using the Taylor series. It can be assumed that the following quantities are replaced by their mean averaged value plus a small perturbation. The mean averaged value is given by a capital letter and the small AC variation is characterized by a lowercase letter and a tilde, see the block of Equation 3.43.

$$d = D + \tilde{d} \tag{3.43}$$

$$i_L = I_L + \tilde{i_L}$$

$$i_{in} = I_{in} + \tilde{i_{in}}$$

$$u_C = U_C + \tilde{u_C}$$

$$u_{in} = U_{in} + \tilde{u_{in}}$$

$$u_{out} = U_{out} + \tilde{u_{out}}$$

In the next step, the terms from the equation blockset 3.43 are substituted into the averaged system equations. After simple algebraic manipulations and the consideration that the derivative of a constant term (I_L) is zero the following equations below are derived.

$$\frac{\mathrm{d}\tilde{i_L}}{\mathrm{d}t} = a_{11} \cdot \tilde{i_L} + a_{12} \cdot \tilde{u_C} + b_{11} \cdot \tilde{d} + b_{12} \cdot \tilde{v_{in}} \tag{3.44}$$

a_{11}, a_{12}, b_{11} and b_{12} represent the following substitution:

$$a_{11} = \left(\frac{R_1 \cdot D + R_2 \cdot D - R_2}{L} \right)$$

$$a_{12} = \left(\frac{R_3 \cdot D - R_3}{L} \right)$$

$$b_{11} = \left(\frac{R_1 \cdot I_L + U_{in} + R_2 \cdot I_L + R_3 \cdot U_C}{L} \right)$$

$$b_{12} = \frac{D}{L}$$

$$\frac{\mathrm{d}\tilde{u_C}}{\mathrm{d}t} = a_{21} \cdot \tilde{i_L} + a_{22} \cdot \tilde{u_C} + b_{21} \cdot \tilde{d} + b_{22} \cdot \tilde{u_{in}} \tag{3.45}$$

a_{21}, a_{22}, b_{21} and b_{22} represent the following substitution:

$$a_{21} = \left(\frac{R_6 - R_6 \cdot D}{C}\right)$$
$$a_{22} = \left(\frac{R_4 \cdot D + R_5 \cdot D - R_5}{C}\right)$$
$$b_{21} = \left(\frac{R_4 \cdot U_C + R_5 \cdot U_C - R_6 \cdot I_L}{C}\right)$$
$$b_{22} = 0$$

Equation 3.46 represents the linearized output system voltage.

$$\tilde{u_{out}} = d_{11} \cdot \tilde{i_L} + d_{12} \cdot \tilde{u_C} - R_7 \cdot I_L \cdot \tilde{d} + c_{12} \cdot \tilde{u_{in}} \tag{3.46}$$

d_{11}, d_{12} and c_{11}, c_{12} represent the following substitution:

$$d_{11} = (R_7 - R_7 \cdot D)$$
$$d_{12} = R_6$$
$$c_{11} = R_7 \cdot I_L$$
$$c_{12} = 0$$

Equation 3.47 represents the linearized input converter current of the energy storage system.

$$\tilde{i_{in}} = d_{21} \cdot \tilde{i_L} + d_{22} \cdot \tilde{u_C} + c_{21} \cdot \tilde{d} + c_{22} \cdot \tilde{u_{in}} \tag{3.47}$$

d_{21}, d_{22} and c_{21}, c_{22} represent the following substitution:

$$d_{21} = D$$
$$d_{22} = 0$$
$$c_{21} = I_L$$
$$c_{22} = 0$$

3.3.8.5 State-Space-Model of the Buck-Boost Converter

The linearized system equations are then transformed into the state space model form which is represented in the below Equations 3.48 and 3.49.

$$\dot{x} = \begin{bmatrix} \frac{\mathrm{d}\tilde{i_L}}{\mathrm{d}t} \\ \frac{\mathrm{d}\tilde{u_C}}{\mathrm{d}t} \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix} \cdot \begin{bmatrix} \tilde{i_L} \\ \tilde{u_c} \end{bmatrix} + \begin{bmatrix} b_{11} & b_{12} \\ b_{21} & b_{22} \end{bmatrix} \cdot \begin{bmatrix} \tilde{d} \\ \tilde{u_{in}} \end{bmatrix} \tag{3.48}$$

$$\vec{y} = \begin{bmatrix} \tilde{i_{in}} \\ \tilde{u_{out}} \end{bmatrix} = \begin{bmatrix} c_{11} & c_{12} \\ c_{21} & c_{22} \end{bmatrix} \cdot \begin{bmatrix} \tilde{i_L} \\ \tilde{u_c} \end{bmatrix} + \begin{bmatrix} d_{11} & d_{12} \\ d_{21} & d_{22} \end{bmatrix} \cdot \begin{bmatrix} \tilde{d} \\ \tilde{u_{in}} \end{bmatrix} \tag{3.49}$$

The represented state space form presents a linear time-invariant model of the converter. The matrix coefficients for the system matrix A, input matrix B, output matrix C and the feed-forward matrix D are assigned to the respective equations. The coefficients are constant values and correspond to the values which are defined in the currently considered operating point. With the use of the state-space-model of the converter system, the transfer function in the frequency domain can be derived. This topic of the transformation from the time domain into the frequency domain can be shown up in Section 3.4. In this section the controller design is finally conducted .

3.3.9 Summary Synchronous Buck-Boost AC-Model

The introduced modeling process is necessary since no actual control IC can control the system during the charging phase. Through the system design phase there is the decision derived that controlling the system through a microcontroller makes sense. With the use of the derived state-space-model different control scenarios can be conducted. However, the question of the best control variable will be still open. Further information of the control engineering part can be viewed in Section 3.4, where the AC model of the converter system is analyzed in different operating points and in different domains. Through the derived theoretical charging process in subsection 3.3.7, in which time-based quantities of the converter signal and the energy storage unit were recorded, all operating points can be described by the state-space-model. In order to be able to control the system, however, the design of the converters storage inductor and MOSFET must first be determined. In Subsection 3.3.12 the dimensioning of the storage inductor is made. In further steps, the design of the final inductor is carried out, see Subsection 3.3.12. Lastly, in Subsection 3.3.14 the MOSFET design is made and analyzed by using the double-pulse-switching-test (DPST) to evaluate its suitability.

3.3.10 Inductor Current Value Calculation

The inductor value calculation is one of the most important design steps when designing a converter system. The inductor is used in this application to transfer the energy from the primary side to the secondary side. Outgoing from the analytical process of the inductor current from Subsubsection 3.3.5 the dimensioning of the inductor is made.

3.3.11 Calculation of Maximal Averaged Inductor Current

In this section, the maximal averaged inductor current is calculated. The aforementioned derivation and linkage with the analytic solution and the steady state analysis of the synchronous buck-boost converter enable this calculation. For the design process the following operating point is defined from Figure 3.13, where the maximum mean averaged inductor current $I_{L,max}$ is given at:

Table 3.8: Maximum operating point parameter list for calculating the maximum acting inductor current

Symbol	Meaning	Type/ Value	Unit
$t_{i_{L,max}}$	Time at maximum inductor current	0.7918	[s]
$U_{in}(t_{i_{L,max}})$	Input voltage	978.76	[V]
$U_s(t_{i_{L,max}})$	Storage voltage capacitor	166.31	[V]
$I_{s,max}$	Charging current storage capacitor	13.59	[A]

The duty cycle at this operating point is calculated by the equation 3.25.

$$D = \frac{U_{out}}{U_{out} + U_{in}} = \frac{U_s}{U_s + U_{in}}$$

Inserting the parameter from Table 3.8 leads to a duty cycle

$$\underline{D = 0.1452.}$$

The calculation of the maximum averaged mean inductor current is done by using Equation 3.27. Instead of applying $\frac{U_{out}}{R}$ fraction term an interchange with the maximum charging current $I_{s,max}$ from Figure 3.5 is made.

$$I_L = \frac{U_{out}}{R} \cdot \frac{1}{1 - D}$$

$$I_{L,max,ave} = \frac{13.59\text{A}}{1 - 0.1452}$$

The maximum averaged mean inductor current is

$$\underline{I_{L,max,ave} = 15.90\text{A}.}$$

Outgoing from the extracted maximum averaged mean current $I_{L,max,ave}$ and the equation of the ripple inductor current 3.28 and under consideration of the specifications in Table 1.3 the inductor can be calculated.

$$L = \frac{U_{in} \cdot D \cdot T_s}{2 \cdot \Delta i_L}$$

By inserting the extracted values for the active acting duty cycle D, the input voltage U_{in} the inductor value L can be calculated. The ripple inductor current is given from the converter specification, see Table 1.5.2.

$$L = \frac{978.7651\text{V} \cdot 0.1452 \cdot 20\mu\text{s}}{2 \cdot 5\text{A}}$$

$$L = 283.85\mu\text{H}$$

The desired selected inductance value for the ongoing inductor design in Subsection 3.3.12 is specified with

$$\underline{\underline{L = 300\mu\text{H}.}}$$

3.3.12 Inductor Design

The calculation of the inductor value in Subsubsection 3.3.11 provides the rich information to finally do the inductance design. The chosen design algorithm is called the K_g-Algorithm. It is an iterative inductor design procedure that is presented by Maksimovic [12]. The algorithm is processed in the following way:

1. Determine core size $K_{g,required}$
2. Determine a suitable core for the specified quantities in Table 3.9 ($K_{g,core}$)
3. Check if $K_{g,core} > K_{g,required}$
4. Determine the number of turns N
5. Determine the air-gap length l_g
6. Evaluate wire size with a spatial investigation
7. Proof the design

For the inductor, design specifications must be defined. The main objective is to avoid saturation of the core material and to obtain an acceptable low DC winding resistance R_{cu}. The design specifications are shown in Table 3.9.

Table 3.9: Design specifications for the storage inductor design

Symbol	Meaning	Type/ Value	Unit
ρ_{cu}	Wire resistivity	$16.8e-9$	$[\Omega\,\mathrm{m}]$
$I_{L,max}$	Peak inductor current	21.5	$[\mathrm{A}]$
L	Inductance	$300e-6$	$[\mathrm{H}]$
R_{cu}	Winding resistance	0.02	$[\Omega]$
F_{cu}	Winding fill factor	0.6	$[]$
B_{max}	Maximum operating flux density	0.2	$[\mathrm{T}]$
f_{sw}	Working Frequency	50	$[\mathrm{kHz}]$
J	Target current density	4	$[\mathrm{A/mm^2}]$
I_{AC}	AC inductor current	5	$[\mathrm{A}]$

1. Determine - $K_{g,required}$

In general the K_g value defines a core geometrical constant and is calculated by Equation 3.50.

$$K_{g,required} = \frac{L^2 \cdot I_{L,max}^2 \cdot \rho_{cu}}{F_{cu} \cdot B_{max}^2 \cdot R_{cu}} \tag{3.50}$$

The required K_g value which needs to be achieved is

$$\underline{K_{g,required} = 1.5e-9.}$$

2. Determine - $K_{g,core}$

The $K_{g,core}$ value combines core geometrical constants of a selected core together and is defined by Equation 3.51.

$$K_{g,core} = \frac{A_e^2 \cdot A_w}{l_w} \tag{3.51}$$

In Table 3.10 the core geometrical constants are shown for a selected core is presented. The core data-sheet values are from TDK-EPCOS-Ferrites-Accessories [31].

Table 3.10: Selected Inductor Core which fulfils the core geometrical constant value $K_{g,required}$

Symbol	Meaning	Type/ Value	Unit
C_{core}	Core type	PM 74/59 N87	[ ]
le	Effective magnetic path length	128	[mm]
A_e	Effective magnetic cross section	790	[mm^2]
A_w	Winding cross section	442	[mm^2]
l_w	Average length of turn	140	[mm]
A_R	Resistance factor	10.9	[µΩ]
A_L	Inductance factor	10000	[nH]
$K_{g,core}$	Core geometrical constant	$1.97 \cdot 10^{-9}$	[ ]
μ_e	Relative effective permeability core	1290	[H/m]
μ_0	Permeability vacuum	$1.256 \cdot 10^{-6}$	[H/m]
$\mu_{r,air}$	Relative permeability air	≈ 1	[H/m]

3. Check if $K_{g,core} \geq K_{g,required}$

The $K_{g,core}$ value of the selected core PM74/59 reaches the required $K_{g,required}$ value.

$$K_{g,core} \geq K_{g,required}$$

$$\underline{\underline{1.97 \cdot 10^{-9} > 1.46 \cdot 10^{-9}}}$$

In order to define now the inductance value L the number of turns around the coil former have to be calculated.

4. Determine Number of Turns - N

The determination of the number of turns N is calculated with Equation

$$N = \frac{L \cdot I_{L,max}}{B_{max} \cdot A_e}. \tag{3.52}$$

The number of turns are specified with

$$\underline{\underline{N = 41.}}$$

5. Determine the Air Gap Length - l_g

In order to achieve the required magnetic inductance factor A_L it is necessary to introduce an air gap in certain applications. In this application an air gap length is mandatory. The air gap calculation is done by using Equation 3.53.

$$l_g = \frac{\mu_0 \cdot L \cdot I_{L,max}^2}{B_{max}^2 \cdot A_e} \tag{3.53}$$

The calculated air gap length is

$$\underline{\underline{l_g = 5.51\text{mm}.}}$$

6. Evaluation of the Wire Size

Under consideration of the target current density J and the resulting skin-effect, a suitable conductor type has to be selected. If further informations about the skin-effect is needed, technical Literature [12] is recommended.

The selected conductor type is shown up in Table 3.11.

Table 3.11: Data-sheet values of the selected conductor of type LF2 500 0.071

Symbol	Meaning	Type/ Value	Unit
-	Conductor	LF2 500*0.071	[ ]
-	Conductor material	Copper	[ ]
-	Conductor type	Braids	[ ]
d_C	Conductor diameter (brutto)	2.3	$[\text{mm}]$
$d_{single,braids}$	Braids diameter	0.071	$[\text{mm}]$
A_C	Conductor cross section	4.15	$[\text{mm}^2]$
N_C	Number of sub-conductors	500	[ ]

The skin penetration depth δ can be calculated with Equation 3.54

$$\delta = \sqrt{\frac{2 \cdot \rho_{cu}}{2 \cdot \pi \cdot f_{sw} \cdot \mu_0}} \tag{3.54}$$

and results with

$$\underline{\delta = 0.2935\text{mm}.}$$

Therefore the effective conductor cross section under consideration of the skin-effect is

$$A_{C,eff} = 1.98\text{mm}^2.$$

The resulting effective current density J_C of the conductor is defined by the AC inductor current I_{AC} and its effective conductor cross-section $A_{C,eff}$.

$$\underline{\underline{J_C = 2.53\mathrm{A/mm}^2}}$$

It can be noted that the current density J_C does not exceed the target current density J. In the final phase of the design process, a spatial investigation is performed to determine if the inductor design together with the used conductor is suitable on the selected core.

Using the Equation 3.55, a spatial investigation is performed to determine whether or not the winding space of the core is sufficient for the designed inductor.

$$A_C \leq \frac{F_{cu} \cdot A_w}{N} \tag{3.55}$$

$$\underline{\underline{4.1548\mathrm{mm}^2 \leq 6.4683\mathrm{mm}^2}}$$

The comparison between conductor cross-section A_C and the winding cross-section A_w gives the result that there is enough space to place the windings. Based on the core geometry this results in about three to four winding layers on the coil former.

7. Proof of the Inductor Design

The last step is now to perform a proof of the inductor design. Outgoing from the data sheet from TDK-Electronics the following core parameters are valid and can be shown up in Table 3.10. The main objective of this part is to analyze whether all design specifications are met or not.

7.2 Inductance - L

The inductance value L proof can be done by using the inductance factor A_L. It must be noted that through the introduction of an air-gap l_g the inductance factor has changed. This means that the core reluctance value R_{core} will be neglected because of its large value. For the inductance value proof, only the air-gap reluctance value R_g is considered.

$$L = A_L \cdot N^2 = \cdot N^2 = \frac{l_g}{\mu_{r,air} \cdot A_e} \cdot N^2 \tag{3.56}$$

$$\underline{\underline{L = 302.62\ \mu\mathrm{H}}}$$

The proof shows that the required inductance value of the design specification are met.

7.1 Winding Resistance - R_{cu}

The winding resistance value R_{cu} is calculated by the resistance factor A_R from Table 3.9 and the number of turns N. Through Equation 3.57 R_{cu} the resistance is calculated.

$$R_{cu} = A_R \cdot N^2 \tag{3.57}$$

The resulting copper winding resistance for frequency $f = 0\text{Hz}$ is

$$\underline{\underline{R_{cu} = 18.32\text{m}\Omega.}}$$

It can be noted that the design specification for the winding resistance R_{cu} from Table 3.9 is met.

7.3 Magnetic Iron Field Strength - H_{fe}

The magnetic field strength H provides rich information about the core saturation level. Through the use of Ampere's law Equation 3.58 the acting magnetic field strength in the iron core H_{fe} can be calculated.

$$\Theta = N \cdot I \tag{3.58}$$

The magnetic field strength equation is then given by

$$H_{fe} = \frac{N \cdot I_{L,max}}{\mu_e \cdot l_g + l_e}. \tag{3.59}$$

The resulting acting magnetic field strength is

$$\underline{\underline{H_{fe} = 121.72\ \text{A/m}.}}$$

7.4 Magnetic Flux Density Iron - B_{fe}

Through the use of the magnetic field strength of the core, the resulting magnetic flux density in the ferrite core is then calculated with 3.60.

$$B_{fe} = \mu_0 \cdot \mu_e \cdot H_{fe} \tag{3.60}$$

$$\underline{\underline{B_{fe} = 197.31\ \text{mT}}}$$

A cross-check with the magnetic hysteresis curve of the N87 core material delivers provides valid evidence, that the inductor design procedure was correctly done.

3.3.13 Summary of Inductor Design

The final inductor parameters for building up the storage inductor in the synchronous buck-boost converter are shown up in Table 3.12.

Table 3.12: Final inductor design parameters of the storage inductor for the synchronous buck-boost converter

Symbol	Meaning	Type/ Value	Unit
-	Core type	PM74/59 N87	[ ]
-	Conductor	LF2 500*0.071	[ ]
L	Inductance	302.62	[µH]
$R_{cu} = R_L$	Copper winding resistance	18.32	$[\mathrm{m}\Omega]$
N	Winding turns	41	[ ]
-	Number of layers	$3-4$	[ ]
l_g	Air-gap length	5.51	$[\mathrm{mm}]$

Through the use of the steady state analysis combined with the analytic calculation the maximum averaged inductor current could be identified. With the use of the K_g-Algorithm the storage inductor which fits best to the desired application is dimensioned and designed. In the next Subsection 3.3.14 the MOSFET design will be presented.

3.3.14 MOSFET Design

The right choice of the semi-conductor is another further important component when designing a converter system. The main target of this section is to select a suitable MOSFET.

The selection of the MOSFET depends mainly on the following parameters:

- Breakdown voltage - $U_{D,S}$
- Drain current rating - I_D
- Low Drain-Source-Resistance - $R_{D,S,on}$
- Gate-Source-Threshold - $U_{GS,th}$
- Gate-Charge - Q_G
- Power dissipation $P_{loss} = I_D^2 \cdot R_{D,s,on}$

The selected MOSFET in Table 3.13 is chosen in dependency of the voltage rating $U_{D,S}$ and its high drain current rating I_D . The voltage rating of $1.2\mathrm{kV}$ is specified for the reason that during turn-off transient the voltage on the drain can reach up to higher values. This happens due to parasitic inductances in the circuit. The maximum rated voltage during the energy recovery process is defined with $U_{in,max} = 1100\mathrm{V}$ which can be seen in Figure 3.3. In this way, it was determined that the maximum applied voltage should be approximately 90% of the rated breakdown voltage which is specified by the manufacturer.

Table 3.13: Final listing of parameters for the inductor design

Component	Specification
MOSFET	Manufacturer: Microchip Technology / Atmel. Silicon carbide (SiC) power MOSFET: MSC080SMA120B. Gate-source threshold: $U_{GS,th} = 1.8\mathrm{V}$. Drain-Source-Breakdown-Voltage: $U_{D,S} = 1.2\ \mathrm{kV}$. Continuous Drain Current: $I_D = 37\ \mathrm{A}$. Drain-Source-Resistance: $R_{ds,on} = 100\ \mathrm{m\Omega}(max)$. Power Dissipation: $P_D = 200\ \mathrm{W}$. Junction to case thermal resistance: $R_{th,j-c} = 0.75°\mathrm{C/W}$

Another criterion for the choice of this transistor is its low gate-source voltage threshold. This leads to the advantage that especially the high-side MOSFET drive control in the H-Bridge can be improved without implementing special drive circuits. Last but not least, this semiconductor is also convincing in that it can carry the required current at given gate-source voltages. The maximum current rating during the energy recovery process is about $22\mathrm{A}$. So in this way, the transfer characteristic ($I_D = f(U_{GS})$) of the transistors current rating is mainly depending on its gate-source voltage. Lastly, its high power dissipation makes them suitable too for this application of energy recovery.

3.3.14.1 Assessment of the Switching Losses

With regard to its suitability, a preliminary calculation is performed using the double-pulse-switching-test (DPST) to evaluate the switching losses of the selected MOSFET under maximum conditions in the charging process [32].

Figure 3.19 presents the schematic circuitry to perform the double-pulse-switching-test. The DPST is conducted in the simulation environment of LTspice.

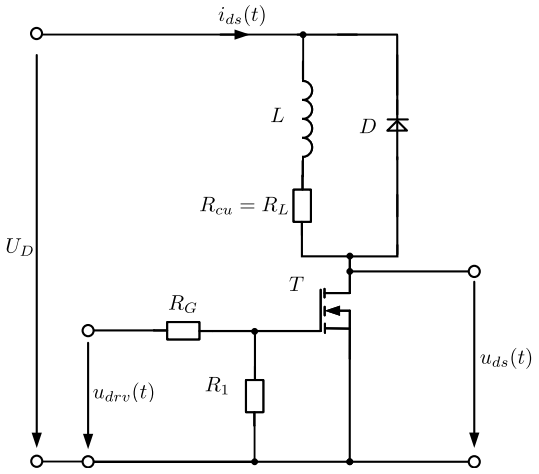

Figure 3.19: Schematic circuit for performing the double-pulse-switching-test in order to analyse the switching losses during on state and off state

The assessment is performed under maximum rated quantity conditions during the energy recovery process. Table 3.14 shows the maximum current and voltage values under which this test is performed.

Table 3.14: Maximum current and voltage values and component values for the double-pulse-switching test

Symbol	Meaning	Value	Unit
T	MOSFET	MSC080SMA120B	[ ]
R_G	Gate resistor	1	$[\Omega]$
L	Storage inductor	302.62	[µH]
D	Flywheel diode	$R_{on} = 0.01$ $U_{fwd} = 2$	$[\Omega]$ [V]
$R1$	Discharge resistor	1000	$[\Omega]$
U_D	Drain voltage	1100	[V]
I_D	Drain current	≈ 21	[A]
U_{drv}	Gate drive voltage	10	V
D	Duty cycle	80	[%]
f_{sw}	Switching frequency	50	[kHz]

The drain voltage corresponds to the maximum input voltage of the synchronous buck-

boost, see Figure 3.3. The maximum drain current is defined by the maximal mean averaged current ($I_{L,max}$) in Figure 3.13 plus its specified ripple inductor current $\Delta i_L = 5\mathrm{A}$. The duty cycle D corresponds to the maximum obtained duty cycle D_{max}, who is given in Figure 3.12. This permits determining the maximum conduction losses.

3.3.14.2 Double-Pulse-Switching-Test Results

In Figure 3.20 the double pulse gate-source drive signal is shown. The falling edge of pulse one $u_{drv}(t)$ defines the OFF-Phase while the rising edge of pulse two defines the ON-Phase.

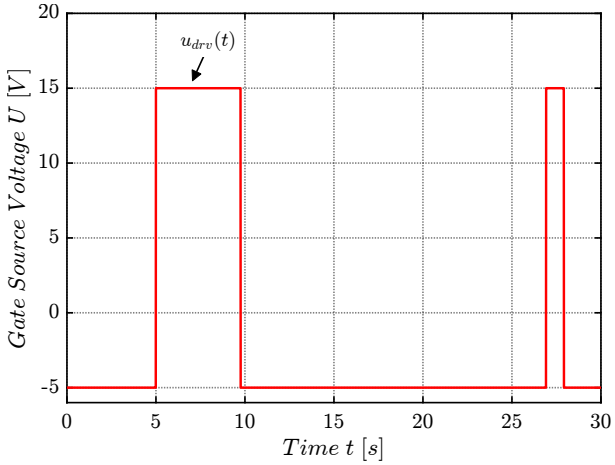

Figure 3.20: Double pulse gate-source drive signal $u_{drv}(t) = u_{pwm}(t)$

The resulting signals of the drain-source voltage $u_{ds}(t)$ is shown in the left diagram while the drain source current is shown in the right diagram of Figure 3.21.

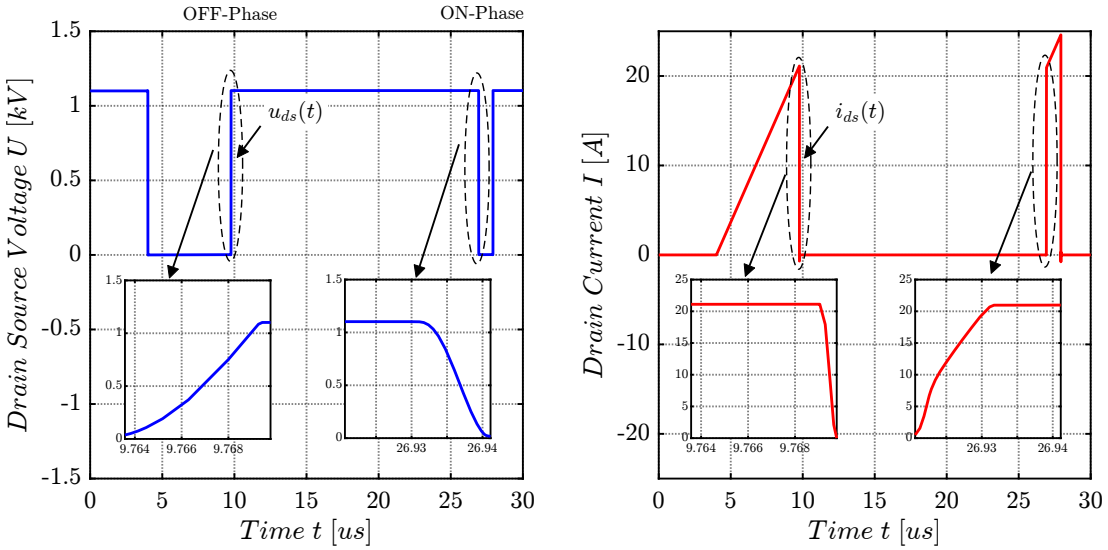

Figure 3.21: Resulting drain-source voltage $u_{ds}(t)$ and drain source current $i_{ds}(t)$ during the double-pulse-switching-test

In the OFF transition phase, it can be seen that the drain-source current has a steep negative current change while the drain source voltage is rising up to its supply voltage U_D. The complete OFF transition time $t_{d(off)}$ is measured with approximately 6ns.

In the ON transition phase the drain-source current and its drain-source voltage behaves similar to the OFF transition but only reversely. The ON transition time $t_{d(on)}$ is measured with approximately 21ns.

In Figure 3.22 the instantaneous power of the ON-Phase and OFF-Phase are shown. The power loss spikes are labelled through the dashed ellipse.

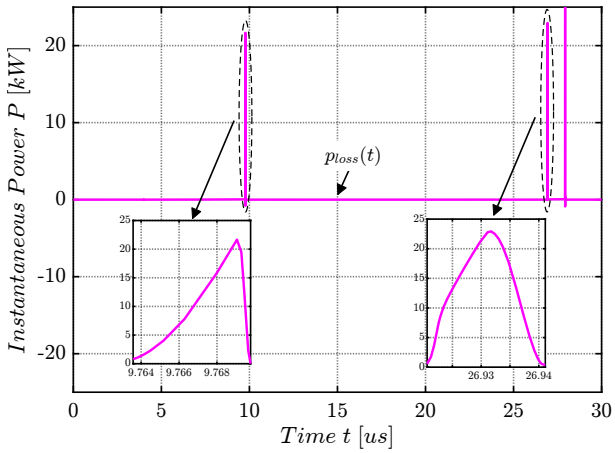

Figure 3.22: Resulting instantaneous power of the ON-Phase (P_{on}) and OFF-Phase (P_{off})

The turn ON energy loss is obtained by

$$E_{on} = \int_0^{t_{d(on)}} u_{ds}(t) \cdot i_{ds}(t)\ dt \tag{3.61}$$

and results for the ON-Phase with approximately

$$E_{on} = 269.40\ \mu\text{J}.$$

The turn OFF energy loss is obtained by

$$E_{off} = \int_0^{t_{d(off)}} u_{ds}(t) \cdot i_{ds}(t)\ dt \tag{3.62}$$

and results in approximately

$$E_{off} = 59.30\ \mu\text{J}.$$

Compared to the data sheet values from the manufacturer, the turn-off energy loss is

slightly greater while the turn-on energy loss is quite higher. However, this is due to the fact that other test conditions are used.

The total power switching losses P_{sw} are obtained through

$$P_{sw} = (E_{on} + E_{off}) \cdot f_{sw}. \tag{3.63}$$

The total switching losses under worst case condition during the charging phase results for a single MOSFET in $P_{sw} = 16.43\ \mathrm{W}$.

In order to specify the conduction losses P_{cond}, the buck-boost converter have to operate in the specified continuous conduction mode. In Figure 3.23 the drain current signal $i_s(t)$ for the continuous conduction mode is shown.

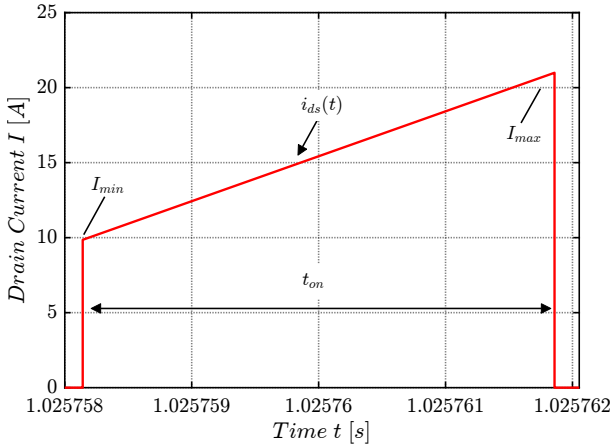

Figure 3.23: Schematic illustration of the drain source current waveform $i_{ds}(t)^{ton}$ during the t_{on} phase of the continuous conduction mode

The maximum ON time for the conduction losses is defined by Equation

$$t_{on} = D \cdot \frac{1}{f_{sw}}. \tag{3.64}$$

By inserting the values from Table 3.14 the maximum on time is derived with

$$t_{on} = 16.00\mu\mathrm{s}.$$

This time defines the maximum occurring on time in the energy recovery proces and therefore also the maximum conduction loss P_{cond}.

The mathematical expression of the drain-source current $i_{ds}(t)$ from Figure 3.23 is given by Equation 3.65.

$$i_{ds} = I_{min} + \frac{I_{max} - I_{min}}{t_{on}} \cdot t \tag{3.65}$$

The maximum conduction energy loss is obtained with

$$E_{cond} = \int_0^{t_{on}} u_{ds}(t) \cdot i_{ds}(t)\ dt = \int_0^{t_{on}} R_{ds,on} \cdot i_{ds}(t)^2\ dt, \tag{3.66}$$

where $i_{ds}(t)$ is the drain source current from Equation 3.65.

The conduction energy loss results with $E_{cond} = 400.53$ µJ

By using Equation 3.67

$$P_{cond} = E_{cond} \cdot f_{sw} \tag{3.67}$$

the maximum conduction loss results with $P_{cond} = 20.02\ \mathrm{W}$.

The total loss $P_{tot,loss}$, under worst case condition of the discharging process, is calculated by

$$P_{tot,loss} = P_{sw} + P_{cond} \tag{3.68}$$

and results with approximately $P_{tot,loss} = 36.45\ \mathrm{W}$.

Outgoing from the total losses during the maximum performance specifications the junction temperature of the MOSFET is calculated. Equation 3.69 shows how the junction temperature T_j is defined. It depends mainly on the case temperature T_c and the thermal resistance between junction and case $R_{th,j-c} = 0.75°\mathrm{C/W}$ (see MOSFET Data-sheet).

$$T_j = T_c + R_{th,j-c} \cdot P_{tot,loss} \tag{3.69}$$

At the present time, no statement can be made about the case temperature during operation. Therefore T_c is simplified with the ambient temperature $T_a = 25°\mathrm{C}$.

The junction temperature results then with

$$T_j = 52.33°\mathrm{C}.$$

According to the manufacturer, the maximum junction temperature shall not reach $175°\mathrm{C}$.

3.3.14.3 Summary MOSFET Design

In conclusion, it can be said that this selection process represents a tool in which the double-pulse-switching-test gives the ability to test power devices under worst case conditions. The mathematical approach and instruction to assess switching losses plus conduction losses are given by Infineon [33]. Especially in the early design stage, this helps to reduce the risk of unforeseen problems, like miss dimensioning. It can be shown, that under maximum working conditions during the energy recovery process, the MOSFET does not exceed the manufacturers power dissipation ($P_{tot,loss} \leq P_D$). But nevertheless, a passive cooling system through a heat sink should be provided for initial hardware purposes. Table 3.15 shows the results of the double-pulse-switching analysis under boundary conditions of the energy recovery process.

Table 3.15: Results of applying the double pulse switching test in order to assess the total power loss for on and off switching

Symbole	Meaning	Value	Unit
E_{on}	Loss energy ON-Phase	269.40	[µJ]
E_{off}	Loss energy OFF-Phase	59.30	[µJ]
P_{sw}	Total switching power losses	16.43	[W]
E_{cond}	Conduction energy losses	400.53	[µJ]
P_{cond}	Conduction power losses	20.02	[W]
P_D	Total power dissipation Manufacturer Data-sheet (at $T_C = 25°\mathrm{C}$)	200	[W]
$P_{tot,loss}$	Total losses	36.45	[W]
T_j	Junction temperature	52.33	[°C]

These obtained simulation results can be stored as reference values. In a required later use for example in the hardware design or during production, this rich information can be seen as a template to evaluate the effects of any kind of modifications. In this current system design process, all components for the construction of the energy storage system have been defined. In addition, a complete analytical calculation of the charging process for intermediate storage of the discharge energy is also available. In the next Section 3.4 the final control engineering design is carried out.

3.4 Control Engineering Design

The control engineering design is the last part of the energy storage system design. Based on the derived small signal averaged model of the synchronous buck-boost converter in Subsection 3.3.8 the controller design can be carried out. Based on the gathered system knowledge, in Subsection 3.4.1 the control variable and the control strategy are defined.

3.4.1 Definition of the Control Variable and the Control System

In accordance with the converter requirements from Table 1.3 the transient power flow on the primary side needs to be transferred in a demand-oriented and controlled manner to the secondary side. In the circuit design of the converter, the storage inductor L was designed according to the criteria of a maximum current carrying capacity. Exceeding the maximum current specifications can lead to saturation effects in the core material. This causes then a decrease in the inductance. Due to the reduction, the inductor current would then carry a higher current ripple and consequently, this can lead then to non permissible component loads. The converter performance depends in this way to a large extent on the inductor current $i_L(t)$.

Moreover from the analytical consideration and the linkage to the converter topology, a direct relationship of a common quantity could be identified. The converter input current $i_{in}(t)$ could be defined as the desired control variable of the energy storage system because it defines a direct relationship between inductor current and discharge power.

On the basis of the defined control variable $i_{in}(t)$ its control transfer function can be analyzed. From the analysis, essential characteristics of the control strategy can be identified. These characteristics will be then taken into account when designing the closed-loop input current control system.

3.4.2 Control Transfer Function Analysis

The dynamic behaviour of the input converter current is analysed with the small signal transfer function from Subsection 3.3.8. In this section the described small signal averaged model for the input current in dependency of duty cycle changes is analyzed. In further context this model is now referred to as the control transfer function $G_{in,d}(s)$, where the index in denotes the input current and d the duty cycle. A schematic representation of $G_{in,d}(s)$ is shown in Figure 3.24.

The control transfer function has two input variables. These input variables are the input voltage U_{in} on the primary side of the converter and the duty cycle D. The first one acts as a disturbance quantity while the second input variable is used to define the ON and OFF time during the power flow control.

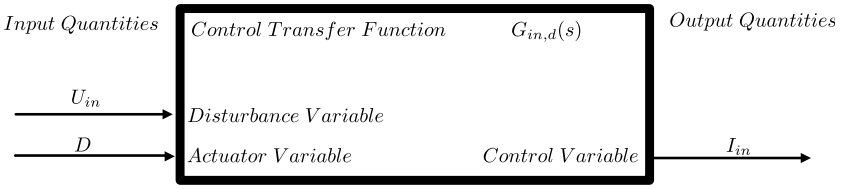

Figure 3.24: Schematic illustration of the considered control transfer function $G_{in,d}(s)$ and its dependencies

3.4.2.1 Time Domain Analysis

The first analysis is considered in the time domain. During the charging process, the system passes different operating points, as it is investigated in Subsection 3.3.8. The aim is to find out whether the operating points remain static with the same dynamic behaviour or whether they differ significantly from each other. The operating points are defined by their steady-state values of the converter analysis and their designed component values L and C_s. In each operating point OP_i, it is assumed that the synchronous buck-boost is driven as a DC-DC voltage converter with a defined load resistance R. In Figure 3.25 ten different operating points along the complete charging process of the input converter current course $i_{in}(t)$ are shown.

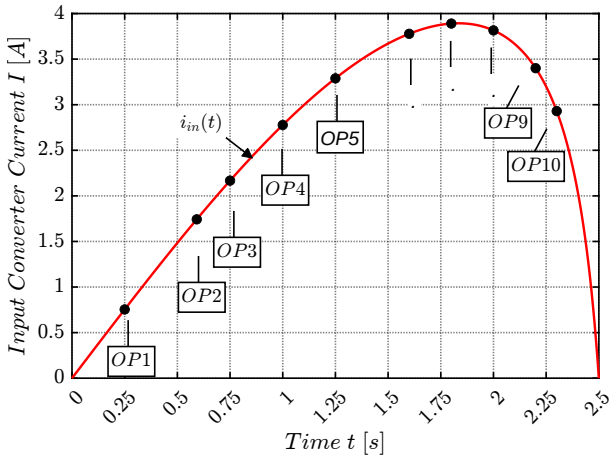

Figure 3.25: Illustration of ten operating points along the complete charging process

The main objective of the time domain analysis is to simplify the subsequent continuous time controller design by only considering three operating points. The choice of the operating points will be defined by observing the system through its Pole-zero map. These three working points should summarize the finite entire space of operating points in the best possible way. The operating point analysis is made by considering ten operating points.

From the previous system design steps following system parameters are known and are listed in Table 3.16. These system parameters were extracted in the course of the system design and are summarized here again.

Table 3.16: System component list of the synchronous buck-boost converter

Meaning	Symbol	Value	Unit
Input source internal resistance	R_{in}	0	[Ω]
Inductor	L	302.62	[µH]
Inductor quivalent series resistance (ESR)	R_L	18.32	[mΩ]
MOSFET drain-source-resistance	$R_{ds,on}$	10	[mΩ]
Energy storage Capacitor	C_s	80	[mF]
Energy Storage Capacitor ESR	$R_{ESR,C}$	3	[mΩ]

In Table 3.16 for each operating point OP_i the load resistance R and its steady-state current and voltage values are given.

Table 3.17: Defined operating points in order to apply the operating point analysis

Operating Point (OP)	t_i [s]	i_L [A]	i_{in} [A]	U_{in} [V]	U_C [V]	D [%]	R [Ω]
OP_1	0.25	10.88	0.73	1087.70	76.55	6.74	7.53
OP_2	0.59	14.96	1.70	1031.60	129.46	11.38	9.76
OP_3	0.75	15.33	2.12	991.00	156.09	13.85	11.81
OP_4	1.00	15.13	2.73	909.01	196.93	18.05	15.88
OP_5	1.25	14.26	3.24	807.11	234.21	22.74	21.25
OP_6	1.60	12.19	3.73	635.82	277.74	30.64	32.84
OP_7	1.80	1.59	3.85	525.77	297.14	36.34	44.03
OP_8	2.00	8.69	3.78	409.01	312.11	43.50	63.53
OP_9	2.20	6.36	3.37	287.38	322.41	53.06	107.97
OP_{10}	2.30	4.91	2.91	225.33	325.81	59.28	162.93

3.4.2.2 Frequency Domain Analysis of Input Converter Current Transfer Function

The second analysis concentrates on the frequency response analysis. In order to this, the state-space-model from Section 3.3.8.5 have to be transformed from time-domain into the frequency domain, by applying linear algebra. Further informations about the use of time to frequency transformation through linear algebra Literature [34] is recommended.

The time to frequency transformation from the derived state-space-model into the Laplace domain is conducted by using the Matlab function $ss2tf()$. The transformation process from time to frequency domain is shown up in Figure 3.26.

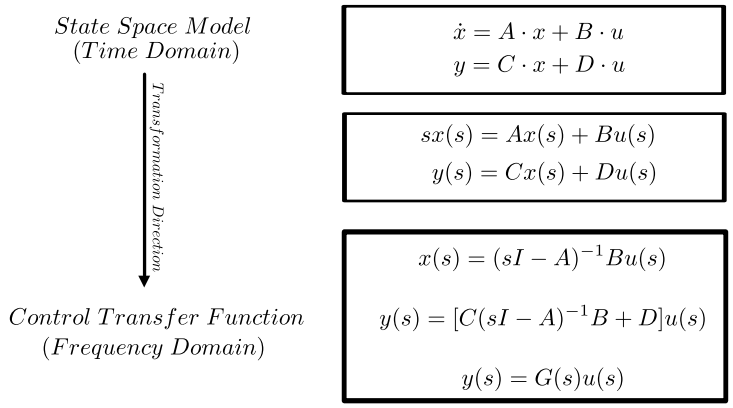

Figure 3.26: Transformation algorithm of state-space-model to control transfer function model [34]

In Equation 3.70 the control transfer function $G_{in,d}(s)$ for a continuous-time system is shown. Such kind of system is also referred to a linear-time-invariant (LTI) system. Here the continuous control transfer function is presented without any uncertainties. The consideration of parasitics have a tremendous influence on the system behaviour, which will be discussed in the sections afterwards. In order to simplify the given transfer function, the numerator here is simplified. This improves the readability. The numerator substitutions are listed directly below and are denoted by a, b and c.

$$G_{in,d}(s) = \frac{a \cdot s^2 + b \cdot s + c}{C_s \cdot L \cdot R \cdot s^2 + L \cdot s + R \cdot (1 + D^2 - 2 \cdot D)} \tag{3.70}$$

$$a = C \cdot L \cdot R \cdot I_L$$

$$b = L \cdot I_L \cdot C \cdot R \cdot D \cdot U_s + C \cdot R \cdot D \cdot U_{in}$$

$$c = R \cdot I_L + D \cdot (U_s + U_{in} - R \cdot I_L)$$

As already analyzed from Subsection 3.3.8 the system is of order two because of two energy-storing elements (L and C). In Figure 3.27 the Bode diagram of the dynamic system model displays the magnitude in dB and the phase in $^\circ$ in dependency of the frequency. The system is defined as a single-input single-output (SISO) model. The input variable is defined as the duty cycle $d(t)$ and the output that responds to a duty cycle change is the input converter current $i_{in}(t)$.

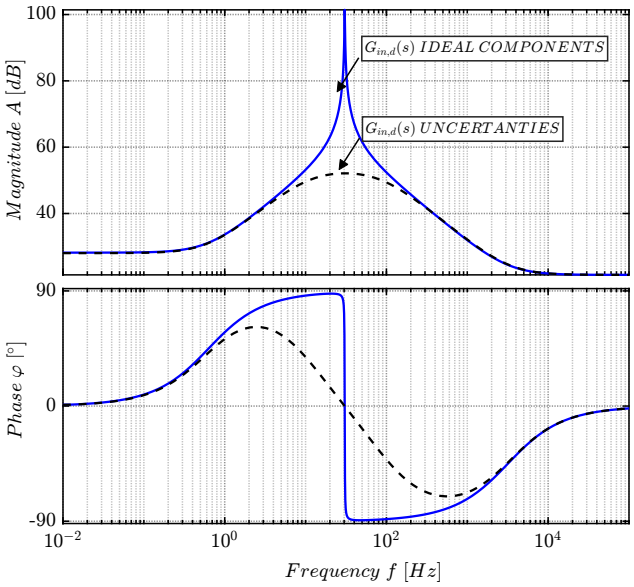

Figure 3.27: Bode diagram of the control transfer function $G_{in,d}(s)$. Operating point- OP_1: $U_{in} = 1087.70$ V and $D = 0.0615$

In the Bode diagram above the blue solid lines depicts the frequency response of the dynamic input converter current model under ideal component conditions. One of the prominent locations is the resonance peak at a frequency of approximately 32Hz. This resonance enhancement is given through the series resonant circuit in which the resonance frequency can be approximately calculated by

$$f = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C}} \, . \tag{3.71}$$

In further analyzation, the dashed black line demonstrates in relation to the blue line no resonant peak. This means that the amplification part is significantly lower at the resonance peak specially. Due to uncertainties, like parasitic components, the oscillation can be attenuated. The maximum amplification depends mainly on the parasitic equivalent series resistance components. These components are causing additional attenuation effects. This is due to the fact that every voltage drop on each resistance reduces the applied voltage to the inductor and so the inductor current slope rate. But in general, it can be mentioned, that the overall gain remains at a high level over a wide range of frequencies. This leads to the following statement, that small duty cycle values results in an extensive change of the control variable $i_{in}(t)$. Additionally at frequencies above 30Hz, the gain drops by 20dB over two decades but stays constant on high gain levels afterwards.

However, compared to the typical applications of DC/DC converters, this converter must be controllable within wide voltage ranges, since the output voltage $u_s(t)$ rises across the charging process, while the input voltage at the converter input $u_{in}(t)$ drops continuously (see Figure 3.4 and 3.3). Therefore, the control transfer function is examined in

further operating points. In Figure 3.28 the comparison of the control transfer function in different operating points is shown.

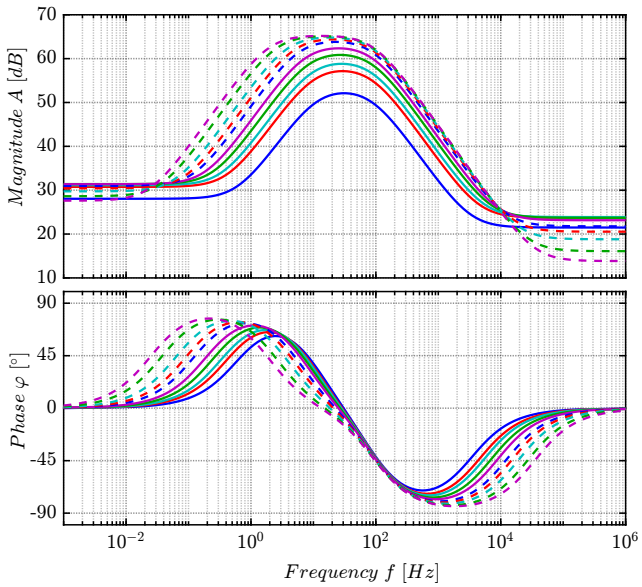

Figure 3.28: Bode diagram of control transfer function under variation of the operating point

Each separate bode line indicates another operating point. The input voltage of the converter is changing in accordance to a quarter period of a sine wave in the second quadrant from $U_{in} = [1100\ \mathrm{V} ... 100\ \mathrm{V}]$. The duty cycle is changing in the range of $D = [0.06\ ...\ 0.8]$. If only the changes of the magnitude is examined, it can be determined that the gain of the control transfer function increases due to the increasing duty cycle. The phase response φ is limited over the total range between $\pm 90\ °$.

In general, an increase of the magnitude due to high duty cycles can cause to destabilize the system. This property must be taken into account in the controller design process.

A further characteristic parameter in the analysation of the control transfer function are gain margin ($[\mathrm{dB}]$) and phase margin ($[°]$). The gain and phase margin are relative measurements and helps to define the stability criteria. In both bode measurements the gain- and phase-margin are infinite. This results that the system is always stable.

3.4.2.3 Step Response and Pole-zero Map

Another time domain analysis is done by using the Step response and Pole-zero map. The step response characterizes the time response of the variable which needs to be controlled. In this case the input current i_{in} of the converter, as a function of the control variable d the input current is stepped out.

In Figure 3.29 the step response of the aforementioned ten operating points are shown. Each step response is stepped out with a unity duty cycle step d. It must be clearly stated that a duty step with a magnitude of one will not be expected during normal operation, it is only for investigation purposes.

The detailed plot diagram in the upper right corner shows up that each transfer function starts at a certain DC-Bias value. This DC-Bias value corresponds to the steady state input current of the converter. This steady state input current is built by the product between the steady state inductor current i_L and its duty cycle D from Table 3.17 (see also Equation 3.34).

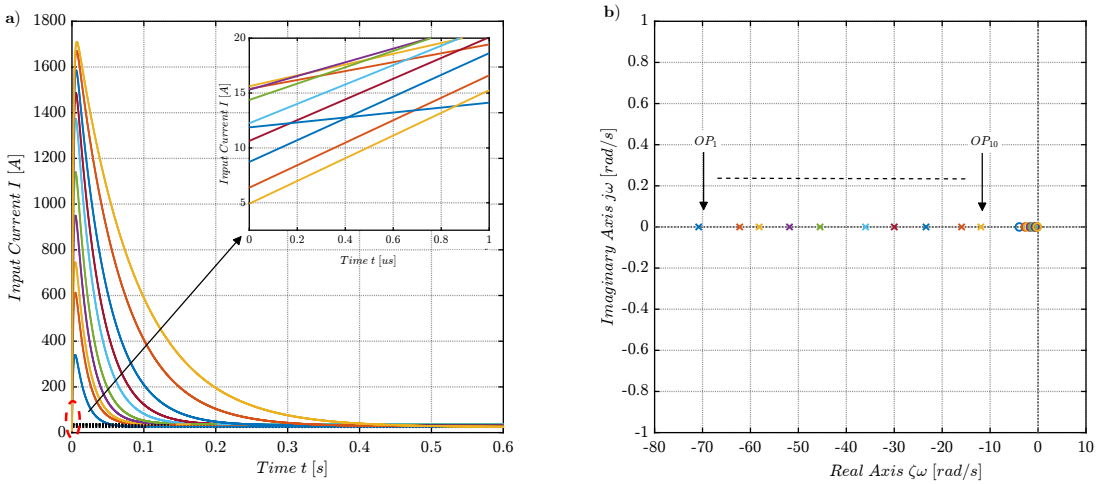

Figure 3.29: Step response data of transfer Function $G_{in,d}(s)$ in ten different operating points when applying a unity duty step

This DC-Bias value is due to the reason that the converter system is actually settled in the current steady state and is then stepped out by a unity duty step $d_{step} = 1$ at time $t = 0\text{s}$.

In Figure 3.29b the Pole-zero map of the control system is illustrated. Outgoing from the Pole-zero map the absolute stability measurements can be defined. In addition, the Pole-zero map mainly defines also the time-based dynamic properties of the system. The presented poles are the dominant poles that mainly influence the time domain properties. The second pole location is located by a factor eight more on the left side and is therefore not as dominant as the presented ones. So in this way, each pole defines a time constant τ_i in the system.

The system with its actual system parameter configuration shows that all poles and zeros are located in the left half-plane wherein a stable system is indicated. In addition, it can be seen that the open loop system is not capable to oscillate. So in this case it can be mentioned that the imaginary part in all operating points is zero and therefore no oscillating behaviour is predicted. This assertion is because the damping ratio ζ is composed as the cosine of the angle ϕ. Since the two poles of the second order system are placed only on the Real-Axis, it indicates that the system is over-damped. The slowest time constant is given for OP_{10} in the system and is about $75\mathrm{ms}$. Another major impact on the time domain characteristics has a decrease of the storage capacitor C or the inductor current L. In this way, the pole location can be influenced tremendously since the system dynamic is getting faster. Figure 3.30 shows schematically the interaction of the pole positions with the characteristic time domain properties values.

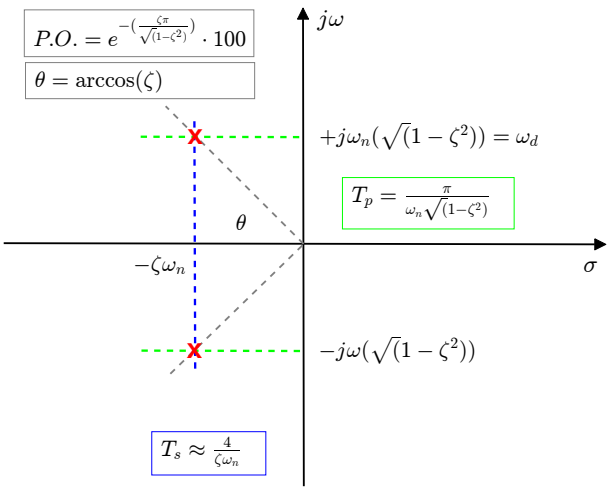

Figure 3.30: Illustration of the Pole-zero map and the characteristic time domain properties

The calculation of the characteristic values like damping ratio ζ or neutral frequency ω_n of a transfer function can be done by the provided equations in Figure 3.30. These equations are also the basis for defining the requirements when applying the root locus method in Subsection 3.4.7 in order to design the controller.

In Table 3.18 the specific characteristic time-based system quantities like damping ratio ζ and neutral frequency ω_n as well as the dominant time constant τ for each operating is shown up.

Table 3.18: Characteristic time domain properties values of the control transfer function in ten different operating points

OP	Pole Location	Zero Location	ζ	ω_n [rad/s]	τ_n [ms]
OP_1	$[-535; -69]$	$[-2.4e4; -3.9]$	1.5	194.6	32.3
OP_2	$[-542; -61]$	$[-3.0e4; -2.7]$	1.6	183.7	34.3
OP_3	$[-546; -57]$	$[-3.5e4; -2.2]$	1.7	178.2	35.3
OP_4	$[-551; -51]$	$[-4.4e4; -1.6]$	1.8	169.1	37.2
OP_5	$[-557; -45]$	$[-5.6e4; -1.2]$	1.9	159.2	39.5
OP_6	$[-565; -35]$	$[-7.7e4; -0.7]$	2.11	142.7	44.0
OP_7	$[-571; -29]$	$[-9.4e4; -0.6]$	2.3	130.9	48.1
OP_8	$[-576; -23]$	$[-1.2e5; -0.4]$	2.6	116.1	54.1
OP_9	$[-583; -15]$	$[-1.7e5; -0.2]$	3.1	96.4	65.1
OP_{10}	$[-586; -11]$	$[-2.2e5; -0.2]$	3.6	83.7	75.1

3.4.3 Summary from the Analysis of the Control Function System Behaviour

In the analysis, the variation of the operating points was always taken into account to get a thorough understanding of the dynamic properties. Various illustrations and analysis tools from frequency response analysis to time response analysis are conducted. In order to do that, the whole charging process was first divided into 10 individual operating points. Stability and behaviour studies were then carried out. The first analysis in the Bode diagram is used to analyze the frequency response of the control transfer function $G_{in,d}(s)$ in an open loop condition. A significant correlation between the control transfer function and the duty cycle was found. With the use of the step response and the Pole-zero map representation, characteristic system parameters like damping ratio ζ or the occurring time constant τ_n were derived.

Outgoing from the analysis of the control transfer function $G_{in,d}(s)$ the following aspects can be summarized:

- The considered open loop transfer function is stable. The control loop is considered to be an optimization to affect the system dynamics, the transient response as well as to compensate for disturbances.
- Due to the application of the buck-boost converter, no right-hand poles are identified.
- The system is characterized as an overdamped system since the damping ratio $\zeta \geq 1$ in all operating points.
- The phase of the analyzed control transfer function $G_{in,d}(s)$ has less than $-90°$ phase shift. Enough phase margin are left over a wide frequency bandwidth.
- The magnitude of $G_{in,d}(s)$ depends on the operating point and thus also on the duty cycle.
- The control functions in operating point one, five and ten are to be used for the controller parametrization. Through the choice of the operating points, an overall characteristic dynamic behaviour of the system is covered.
- The averaged time constant of the system is approximately $46.5\mathrm{ms}$. The time constant τ delivers important information about the system response time.

3.4.4 Determination of the Control Structure

In the present controlled system with a phase shift of less than $-90\,°$, the bandwidths of the filter will limit the controller bandwidth. Therefore, a proportional integral controller (PI) is sufficient for the given application.

For the further controller design process, the following basic analog control loop system in Figure 3.31 will be considered. The main task of this control loop is to affect the plant in that way that the control variable $y(t)$ follows the reference variable $r(t)$. Let in this application $r(t)$ the input reference converter current $i_{in,ref}(t)$ and $y(t)$ the present input converter current $i_{in}(t)$ at the output. The presented control system also illustrates disturbance variables that are acting directly on the controlled system (Plant). These disturbances can be, for example, the parameter variation of the components, due to thermal stress. This then leads to a change in the dynamic behaviour of the controlled system in the further course.

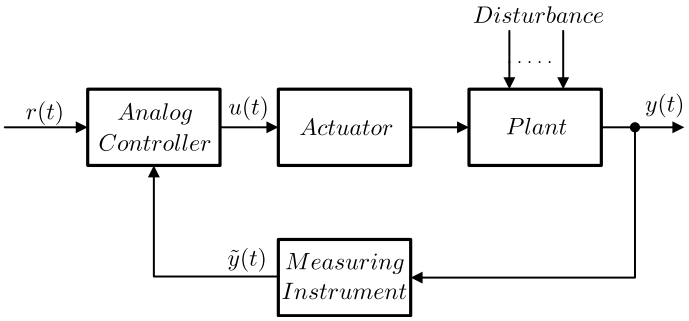

Figure 3.31: Schematic representation of the analog closed-loop control scheme

Through a measuring instrument, the control variable $i_{in}(t)$ in the feedback path is measured. The measurement quantity $\tilde{y}(t) = \tilde{i_{in}}(t)$ of the control variable is then compared with the reference variable. The analog controller provides in a suitable manner then the actuator variable $u(t) = d(t)$ to the controlled system, in order to rule out deviations. In Figure 3.32 the PI-Controller in its general parallel configuration is shown.

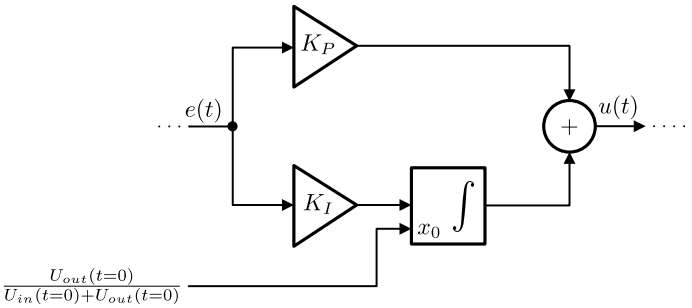

Figure 3.32: Schematic representation of the PI-Controller with an initial condition x_0 initialization in order to avoid inrush current peaks

In addition, the PI-Controller reduces the phase response of the open loop by 90°

for low frequencies and leads to an amplification of $20\ \mathrm{dB}$ per decade. In the high-frequency bandwidth, the phase response is not changing. The control loop amplification is amplified by K_P. The initial value for the integrator corresponds to the duty cycle D of the converter in its steady state condition at discharge time $t_{dis} = 0\mathrm{s}$.

But to carry out the control of the energy storage system (ESS) in a practical sense, the analog closed-loop control scheme has to be transferred to a digital control system. In Figure 3.33 the digital closed loop control structure is shown up. The dashed line box highlight and separates the digital segment from the analog part.

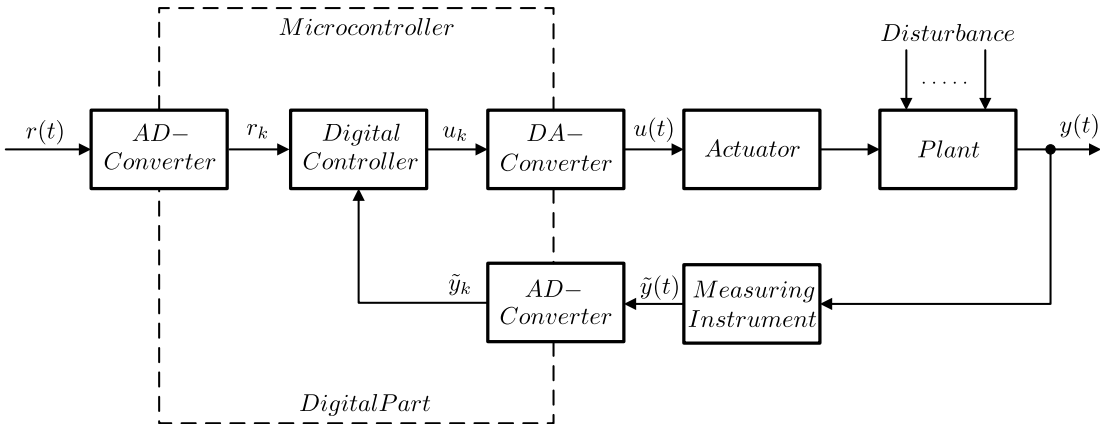

Figure 3.33: Schematic representation of the digital closed-loop control scheme where the dashed line highlights the digital part

Those quantities from the analog segment like input converter current $i_{in}(t)$ must be now analog to digital converted by ADC. This quantity is then only available at certain time stamps $t = k \cdot Ts$. This means in conclusion that the actuator variable $u(t)$ is only updated at this time.

In the ongoing system design, the control variable is defined with the input converter current $i_{in}(t)$. These quantity stays in direct contact with the available power flow on the primary side of the converter and makes them suitable for the desired application.

Before the PI controller design can be conducted the current sensing design has to be carried out. In Subsection 3.4.5 the idea of the sensing design is described.

3.4.5 Current Sensing Design

In order to measure the input converter current, a sensing system is necessary. Through the aid of a $15\ \mathrm{m\Omega}$ shunt resistor the current is converted into an equivalent voltage. This voltage is then filtered by a filter stage to build up an averaged value out of the switched current signal. A differential operational amplifier circuit amplifies the output filter signal and makes it available for the analog to digital conversion. The current sensing scheme is demonstrative shown in Figure 3.34.

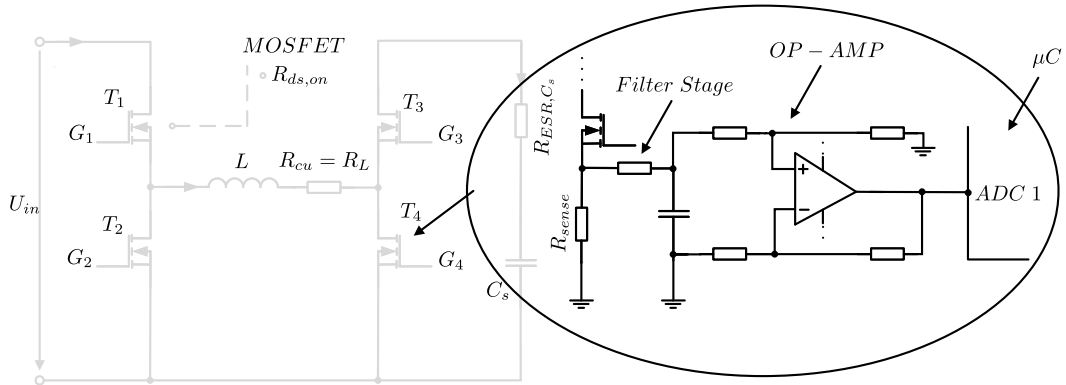

Figure 3.34: Schematic representation of the input current measurement sensing concept

3.4.6 Filter Design

In Subsection 3.4.5 a schematic representation of the sensing concept is demonstratively shown. The current sensing design consists of a sensing stage, a filter stage and an amplification stage.

The filter design in stage two of the sensing scheme is a crucial design process, when trying to control the input current $i_{in}(t)$. In Figure 3.35 the unfiltered input converter current $i_{in,unfiltered}(t)$ is schematically shown in comparison to the filtered input converter current $i_{in,filtered}(t)$. It can be seen that through the switching cycles in the second switching phase $(1 - D) \cdot T_{sw}$ no input current is flowing. So let's consider a scenario where the analog to digital converter (ADC) would sample at a timestamp where the input current is still zero. If this would happen, then in further consequence a huge error $e(t)$ will be expected. Afterwards a huge actuation must be taken by the PI-Controller to counteract. In order to avoid this, a low pass is implemented.

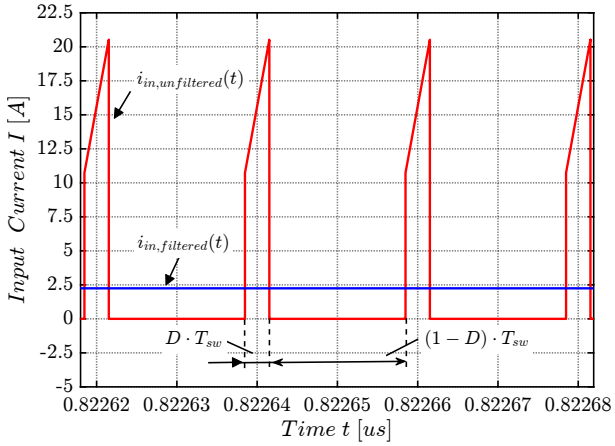

Figure 3.35: Schematic illustration of the unfiltered and the filtered input converter current $(i_{in,unfiltered}(t),\, i_{in,filtered}(t))$

The characteristic filter settings like filter order as well as the filter cut-off frequency f_c needs to be chosen according to the application.

In order to keep things simple for a better understanding, a passive low-pass filter of the order first is chosen. The low pass filter has the following settings, which can be looked up in Table 3.19.

Table 3.19: Low-pass filter settings for the current sensing concept

Symbol	Meaning	Value	Unit
-	Filter Order	1	[ ]
-	Slope-Attenuation	20	[dB/*decade*]
f_c	Cut-off Frequency	≈ 1.5	[kHz]
R_{LP}	Low pass resistor	1	[kΩ]
C_{LP}	Low pass capacitor	100	[nF]

The control transfer function of the low-pass filter $G_{LP}(s)$ is given with

$$G_{LP}(s) = \frac{1}{R_{LP}C_{LP}s + 1}. \tag{3.72}$$

To complete the whole sensing system, a differential amplifier is necessary to amplify the measured signal to the analog-digital reference voltage of the microcontroller. In the next Subsection 3.4.7 the analog continuous closed-loop input current controller design can be carried out.

3.4.7 Continuous Closed-Loop Input Current Control System of Synchronous Buck-Boost Converter

In this subsection, the closed-loop input current control of the synchronous Buck-Boost converter for controlling the power flow from the primary to the secondary side is presented. The choice of the controller has been made after the analysis of the control transfer function $G_{in,d}(s)$ is made. The result is, that a PI-Controller is sufficient for the given application. The design process of the PI-Controller is done by designing first an analog controller. After the controller meets the performance specification the digital controller is emulated by the analog controller.

In order to design an analog controller, time domain specifications have to be defined at first. In Table 3.20 following specifications for the closed control loop system are defined. These specifications have to be met by the control structure.

Table 3.20: Time domain specifications for the closed-loop control system

Percentage Overshoot $P.O.$ [%]	Settling Time T_{set} [ms]
35	5

The settling time is defined as the time which is required for the output to reach a steady-state value within a given tolerance band. The given tolerance band is defined by plus minus two percent.

The analog PI-Controller is designed on the basis of operating points OP_1, OP_5 and OP_{10}. In Table 3.17, from chapter 3.4.2 the operating point are shown up. The reason for choosing these three operating points is that they take all other operating points into account as well.

The controlled transfer function $G_{in,d}(s)$ from Subsection 3.4.2 describes the small signal averaged model of the input current in dependency of duty cycle changes in the respective operating point. In Subsection 3.4.3 a summary of the most important findings about the dynamic of the control transfer function behaviour is given.

In order to adapt a better control of the overall energy storage system, the transfer function $G_{in,d}(s)$ is extended with the transfer function of the filter $G_{LP}(s)$. The following transfer function for the controller design have to be considered further,

$$G_s = G_{in,d}(s) \cdot G_{LP}(s). \tag{3.73}$$

This Subchapter defines now the main part of the control engineering design. It defines the design procedure of the PI-Controller.

The continuous time PI-Controller can be expressed in the time domain with Equation 3.74.

$$u(t) = K_P \cdot e(t) + K_I \cdot \int_0^{T_s} e(\tau)\, d\tau \tag{3.74}$$

Let $u(t)$ the actuator output quantity, $e(t)$ represents the error between reference signal and measured signal, K_P the proportional gain constant and K_I the integral proportional gain constant. In the current system the control output $u(t)$ is given as the duty cycle $d(t)$.

The transfer function of the PI-Controller is given by

$$C(s) = \frac{U(s)}{E(s)} = \frac{\mathcal{L}\{u(t)\}}{\mathcal{L}\{e(t)\}} = \frac{K_P \cdot s + K_I}{s}. \tag{3.75}$$

The controller design is conducted by using a computer-aided interface which is called system designer in Matlab. With this graphical user interface the PI-compensator is designed based on the root-locus method. The specification to meet the time response requirements for the closed-loop system can be defined in Figure 3.30. In Figure 3.36 the computer-aided controller design interface is shown. In this figure the yellow areas indicates the spatial area in which the time domain specifications are not met. Through the use of the below state formulas these restriction areas can be calculated.

The percentage overshoot is given with Equation 3.76.

$$P.O. = e^{-\left(\frac{\zeta \cdot \pi}{\sqrt{1-\zeta^2}}\right)} \leq 35\% \tag{3.76}$$

Through some simple algebraic modification a changeover to the damping ratio ζ is made. By inserting the percentage overshoot the final to achievable damping ratio ζ is defined.

$$\zeta \geq \frac{-ln\left(\frac{P.O.}{100}\right)}{\sqrt{\pi^2 + ln^2\left(\frac{P.O.}{100}\right)}} \geq 0.31$$

The necessary range restriction to obtain the settling time requirement is given by equation

$$\zeta\omega_n = \frac{4}{T_{set}} \tag{3.77}$$

$\zeta\omega_n$ defines then the vertical line restriction in the root locus plane.

The final PI-control design is made by using the control transfer function of operating point one $G_{OP1}(s)$. The reason why operating point one (OP_1) is used, has to do with its dynamical behaviour. In comparison to all other operating points from Table 3.17, the operating point one shows the highest overall dynamic due to the greatest neutral

frequency ω_n. By a smart placement of the PI-Controllers zero, a root locus modification is made. This has the consequence that the trajectory of the root locus curve change. By this kind of modifying the system pole trajectory, the transfer function can be shifted into permissible time ranges through the proportional gain K_P adjustments.

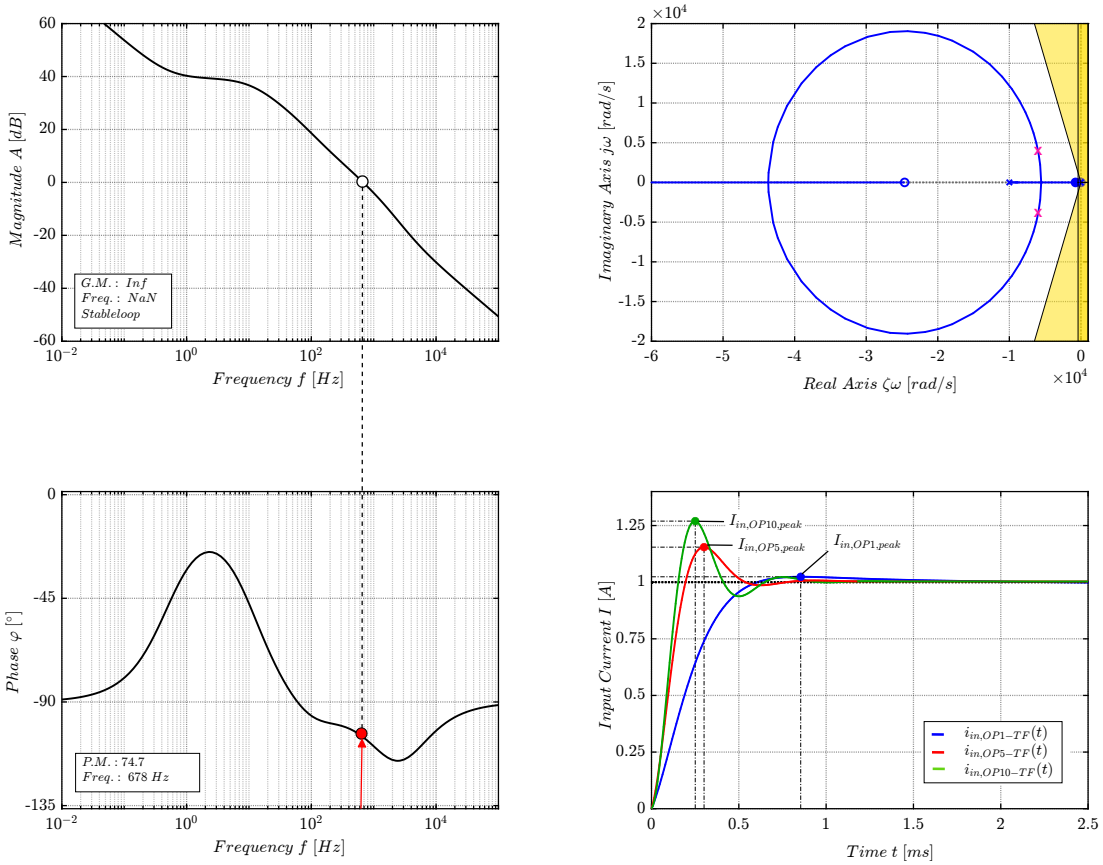

Figure 3.36: Control system designer interface in Matlab when apply the root-locus method for designing a continuous PI-Controller

Finally in subplot four of Figure 3.36 the closed-loop step response of operating one, five and ten is shown.

When the time response characteristics meets the requirements in all three considered operating points, a coefficient comparison has to be performed for getting the control parameter K_P and K_I. The final PI parameter are listed in Table 3.21. The integration time T_I of the controller is quite faster than the time constant of the fastest control transfer function. The integral time is calculated by

$$T_I = \frac{K_P}{K_I} \tag{3.78}$$

and defines a physical quantity of the integrator. In addition, the an initial integral condition x_0 is defined.

The objective was to modify the dynamics of the control transfer function $G(s)$ in that way that all working points meet the time domain specifications.

Table 3.21: Parametersettings of the designed PI-Controller

Symbol	Attribute	Value	Unit
K_P	Proportional Gain	$16.89e-3$	[]
K_I	Integral Gain	12.79	[]
T_I	Integration Time	≈ 1.3	$[\mathrm{ms}]$
x_0	Initial Integral Condition	$x_0 = \frac{U_{s,out}(t=0)}{U_{in}(t=0)+U_{s,out}(t=0)}$	[ ]

3.4.8 Summary of the Continuous Closed-loop Input Current Control System

In this very extensive chapter the whole control engineering design whit an analysis of the open loop control transfer function $G(s)$ is made. The analysis of the controlled system was necessary for getting a thorough understanding about the system behaviour. Through the main summarized characteristic properties of the open loop control transfer function three operating points were considered for the controller design. With the use of the system designer in Matlab which is a computer-aided design interface the PI-Controller was conducted. The controller design is carried by applying the root-locus method. The final PI-Controller settings are displayed in Table 3.21. As a next step a discrete version of the continuous time controller $C(s)$ has to be emulated. The emulation process is carried out in the next Subsection 3.4.9.

3.4.9 Discretization of the Continuous-time PI-Controller

In order to define the digital PI-Controller the analog PI-Controller has to be emulated.

The PI-Controller is defined in time domain by the Equation 3.79.

$$u(t) = K_P \cdot e(t) + K_I \cdot \int_0^{T_s} e(\tau)\, d\tau \tag{3.79}$$

The transfer function of the PI-Controller in the Laplace domain is demonstrated by Equation 3.80.

$$C(s) = \frac{U(s)}{E(s)} = \frac{\mathcal{L}\{u(t)\}}{\mathcal{L}\{e(t)\}} = \frac{K_P \cdot s + K_I}{s} \tag{3.80}$$

Through some mathematical modifications the following differential equation below is obtained.

$$u(kT_s) - u((k-1)T_s) = K_P \cdot e(kT_s) - K_P \cdot e((k-1)T_s) + K_I \cdot \int_{(k-1)T_s}^{kT_s} e(\tau)\, d\tau \tag{3.81}$$

The integral in Equation 3.81 it then numerically approximated by the trapezoidal rule.

The trapezoidal rule is given by Equation 3.82.

$$\int_{(k-1)T_s}^{kT_s} e(\tau)\, d\tau = \frac{T_s}{2}\,(e_{k-1} + e_k) \tag{3.82}$$

Equation 3.83 finally represents the emulated discrete PI-Controller which can be then implemented into the modelbased hardware design of the energy storage system.

$$u_k = u_{k-1} + \left(K_I \cdot \frac{T_s}{2} + K_P\right) \cdot e_k + \left(K_I \cdot \frac{T_s}{2} - K_P\right) \cdot e_{k-1} \tag{3.83}$$

A detailed derivation from Equation 3.79 to the difference Equation 3.82 can be found in the technical literature [35] and [36]. In the next Section 3.5 the energy storage system will be modelled in a hardware near implementation.

3.5 Model-Based Hardware Implementation

The model-based hardware implementation depicts the final system of the energy storage system. Through the taken effort in different technical areas, a complete setup of the system can be defined.

The final energy storage system is implemented in Matlab Simulink with Plecs Blockset. A complete system block diagram in Figure 3.37 shall give a detailed disclosure of the model-based hardware implementation.

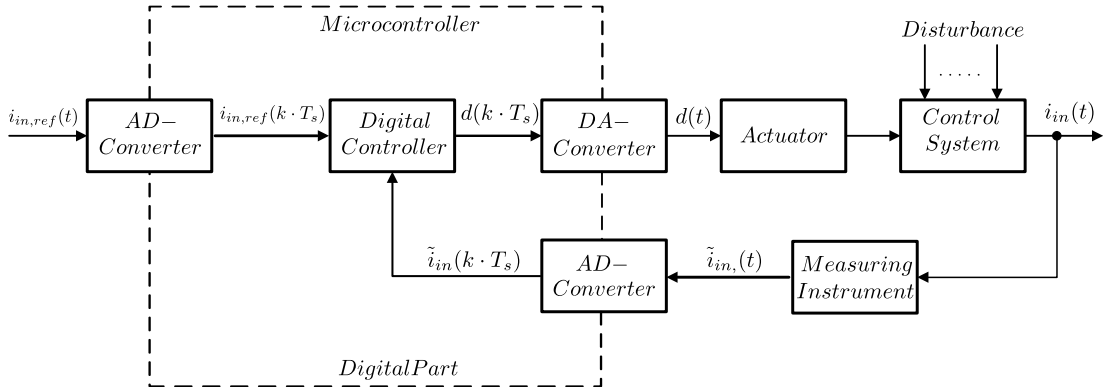

Figure 3.37: Big picture of the final discrete energy storage system in block diagram form

In the next paragraphs, the individual blocks from Figure 3.37 are now assigned and described in more detail.

The control system block builds the most important link in the energy storage system and describes the synchronous non-inverting buck-boost converter with its energy storage unit. It is built up with its parasitic components and shall bridge the gap closer to the real hardware. Further description of the converter topic can be found in 3.3. The complete design process for the energy storage unit is readable in Section 3.1. A bill of material for a laboratory setup for a later development phase is listed in Subsection 3.5.1.

The current sensing concept can be looked up in Subsection 3.4.5. The measuring unit itself contains of a low-side shunt resistor R_{sense} for measuring the input converter current $i_{in}(t)$. A filter stage is used to get the averaged input converter current. A current sense amplifier is utilized that amplifies the sensed current voltage in order to make the control signal useable for the ADC. The filter is composed as a low-pass filter of the first order. A differential amplifier is established as an amplifier. Furthermore a voltage divider is used to sense the input converter voltage $u_{in}(t)$.

The AD-converter stage defines the conversion from the analog domain to the digital domain. This part is usually done with a microcontroller. The modeled ADC consists in the simulation of a sampling unit and a discretization unit which is shown in Figure 3.38. The sampling is established with a zero-order-hold block where the sampling period is

defined with $T_s = 0.1\text{ms}$. With the aim of a 12-bit ADC resolution ADC_q the sampled signal is quantized. The saturation blocks defines the limits in order to saturate over voltages. The ADC reference voltage is defined with $U_{ADC} = 3.3\text{V}$.

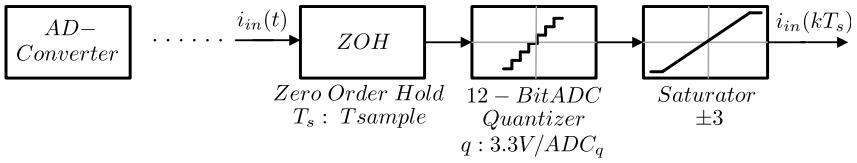

Figure 3.38: Analog to digital converter

The digital to analog conversion of the actuator signal $d(k \cdot T_s)$ is not applicable in the current system. The reason is that the calculated duty cycle value of the digital controller is directly linked to the microcontroller pulse-width-modulation (PWM) unit. In the simulation the PWM unit is given by a relational operator that compares the actual duty cycle with the triangular wave, see Figure 3.39. The output of the PWM unit defines the input gate-source drive signals for controlling the synchronous converter in its buck-boost operation mode.

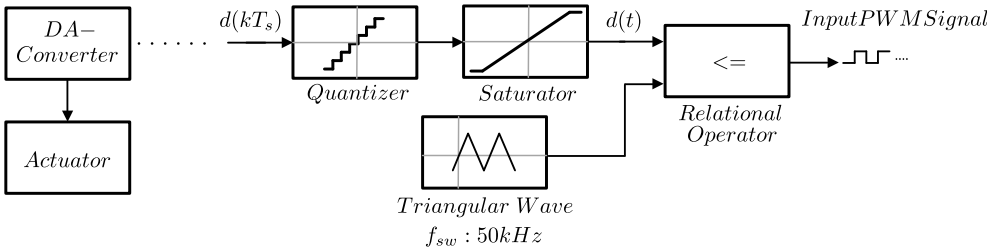

Figure 3.39: Pulse-width-modulation unit which represents hardware gate-driver IC

With the use of a so called C-Script block the implementation of a custom digital controller is carried out. The C-Script block allows the use of the advanced capabilities of the C programming language and combines the flexible sample time settings in order to develop any custom component model. In order to interface the C-Script in the simulation engine, a number of function calls must be predefined.

The digital control law by using discrete time states is build up in Listing 3.1, where the update function call for the controller is realized by implementing the discrete difference equation from Subsection 3.4.9. The digital control algorithm will be retrieved in a separate 10kHz timing sequence. Further informations about the C-Script block Reference [37] is recommended.

$$u_k = u_{k-1} + \left(K_I \cdot \frac{T_s}{2} + K_P\right) \cdot e_k + \left(K_I \cdot \frac{T_s}{2} - K_P\right) \cdot e_{k-1}$$

Listing 3.1: Pseudo code description of the PI controller of the energy storage system

```
// Defination of  PI-Control Algorithm in the update function handler
// of the C-Script block:

//Differenz Equation extracted through an emulation process
uk = uk_1 + (Ki*Ts/2 + Kp)*ek + (Ki*Ts/2 - Kp)*ek_1;


// Anti-Wind-Up Strategy
if(uk >= 0.05 && uk <= 0.95)
{
OutputSignal(0,0) = uk;
}
else if (uk <= 0.05)
{
OutputSignal(0,0) = 0.05;
}
else if (uk >= 0.05)
{
OutputSignal(0,0) = 0.95;
}


// The OutputSignal corresponds to the duty cycle d(t).
```

In addition to the PI-Controller strategy an anti-wind-up strategy is implemented through a saturator function. The saturation function in Equation 3.84 describes its used case range for the actuator signal $d(t) = pwm$.

$$u_{satt}(pwm) = \begin{cases} 0.95, & pwm > 0.95 \\ pwm, & 0.05 \leq pwm \leq 0.95 \\ 0.05 & pwm < 0.05 \end{cases} \tag{3.84}$$

This improves the control characteristics and eliminates wind-up effects. If these effects would be allowed, this would cause an additional dead time T_{dead} in the control system. In a further consequence, the PI-Controller is then inactive and in a later time step the system gets incapable of control. As a result, the integrator must lower in the first instance the integral part. At the same time, however, the reference variable can change further, either in favor for the integrator or, in the worst case, to a further integration.

The last part of the implementation concerns the synchronized sampling strategy. In Figure 3.40 the sampling strategy for a synchronized input current sampling is illustrated. The third figure shows the PWM signal $u_{pwm}(t)$. Let $u_{pwm,sample}(t)$ be defined as the half of the duty cycle $d(t)$.

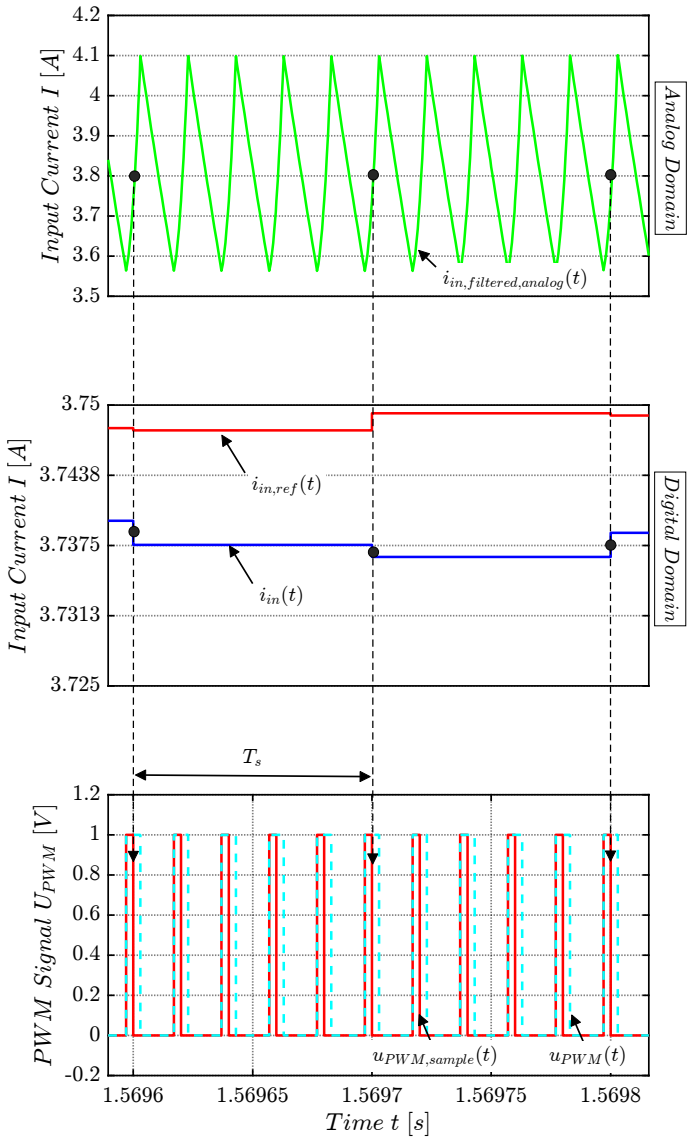

Figure 3.40: Schematic illustration of the sampling concept of the input current $i_{in}(t)$ for synchronous sampling when every fifth switching cycle follows

In this way, whenever a falling edge of $u_{pwm,sample}$ is detected an event is triggered and an ADC conversion of $i_{in}(t)$ is made. The sampling strategy shall be implemented in a timer interrupt-service-routine (ISR). Only every fifth sample value have to be used in order to meet up the sampling frequency f_s. The first diagram represents the analogues filtered input current while the second diagram illustrates the digitized input current in the digital domain. Further on, the sampled data is feed forwarded to the timer routine of the control algorithm. The PI-Controller will be actualised every sample period $T_s = T_{sample}$. In this way, the whole control loop is closed in their structure and extensive sensing and sampling concept supports a stable control process.

3.5.1 Bill of Material

Table 3.22 lists all components that were captured and sized during the design process for the power control stage.

Table 3.22: Compilation of the energy storage system components used for the laboratory sample

Component	Specification
Inductor	Ferrite Core *PM74/59*: Permeability: 1290 AL-Value: 180nH Material: N87. Number of turns are 41 with stranded wire (LF2 500*0.071). The calculated inductance value at maximum current: $300\mu\mathrm{H}$. Air Gap: $5.5\mathrm{mm}$. The calculated copper winding resistance: $R_{cu} = 18.32\mathrm{m}\Omega$
MOSFET	*Microchip Technology / Atmel: MSC080SMA120B:* TO-247 Package. Total Power Dissipation: $200\mathrm{W}$. Four MOSFETs have to be in use due to H-Bridge configuration.
Energy-Storage-Capacitor	*Kemet: ALS71H203QT400:* Aluminium Electrolytic Capacitor. Rated Capacitance $20000\mu\mathrm{F}$. Rated DC-Voltage $400\mathrm{V}$. Ripple Current $37.9\mathrm{A}$. Equivalent Series Resistor $R_{ESR} = 12\mathrm{m}\Omega$.

Gate-Driver IC and Auxiliary power supply

The H-Bridge is controlled with two half-bridge drivers, of type UCC21220 from TI. This driver can be used in applications like solar inverter, industrial transportation and or robotics. The used driver IC supports two PWM inputs. The external boot-straping concept permits high-side MOSFET control. For the running operation a $15\mathrm{V}$ power supply is required. This is realized by a DC-DC converter from Traco-Power, type TRN3-1213.

Table 3.23: Compilation of the peripheral components for the buck-boost converter in order to control the H-Bridge

Component	Specification
Gate-Driver	Half Bridge Driver: *Texas Instruments: UCC21220: Package:* SOIC-16. Supports up to $18\mathrm{V}$ Ouput Drive Voltage. TTL and CMOS compatible inputs. Isolated and have a high noise immunity.
DC-DC-Converter	Isolated DC-DC-Converter: *Traco: TRN3-1213:* Input voltage range from $9\mathrm{V}$ up to $18\mathrm{V}$. Output voltage $15\mathrm{V}$. Ouput current $200\mathrm{mA}$. Output Power $3\mathrm{W}$.

Control and Current Measurement

In Table 3.24 the necessary components and for the control system and the sensing scheme are presented.

Table 3.24: Compilation of the components used for the laboratory sample for the synchronous buck boost converter

Component	Specification
Current-Sense-Resistor	Sense-Resistor: *Ohmite: FCSL150R015FER:* Resistance $15\mathrm{m}\Omega$. Deviation tolerance 1%. Rated Power $10\mathrm{W}$.
Filter Stage	Low-pass filter: $R_{LP} = 1000\mathrm{Hz}$. $C_{LP} = 100\mathrm{nF}$ $(X7R)$. First order. Break-frequency $1591.5\mathrm{Hz}$. $20\mathrm{dB}/decade$.
Current-Sense-Amplifier	*Texas Instruments: INA180:* Gain option $50\mathrm{V/V}$. Common-mode range $-0.2\mathrm{V}$ to $+26\mathrm{V}$. Offset voltage $\pm 150\mu\mathrm{V}$. Output slew rate $2\mathrm{V}/\mu\mathrm{s}$.
DC-DC-Converter	Isolated DC-DC-Converter: *Traco: TRV 1-1511M:* Input voltage range from $12\mathrm{V}$ up to $18\mathrm{V}$. Output voltage $5\mathrm{V}$. Ouput current $200\mathrm{mA}$. Output Power $1\mathrm{W}$.
Voltage- Divider	$R1 = 10\mathrm{M}\Omega$ and $R_2 = 27\mathrm{k}\Omega$. Rated power $0.25\mathrm{W}$.

In order to maintain the required charging profile based on the power flow, a control system is required. A $18\mathrm{m}\Omega$ measurement shunt with a resistance tolerance of 1% and power rating of $10\mathrm{W}$ is used. The filter stage is composed by $1\mathrm{k}\Omega$ resistor and a $100\mathrm{nF}$ capacitor. A classical difference amplifier topology is used to is used to amplify the filtered current voltage values towards to the full ADC reference voltage range. In order to this an INA180 current sense amplifier with gain option (G=50) is used. Compared to a widely used op-amp such as the LM321, the INA180 features a maximum offset of $150\mu\mathrm{V}$. A $350\mathrm{kHz}$ bandwidth and a $2\mathrm{V}/\mu\mathrm{s}$ slew rate makes the INA180 quickly in tracking input current changes. A DC-DC converter supplies the current sense amplifier. To isolate the measurement of the voltage drop of the input current in the power stage caused by the shunt resistor, differential signal acquisition is recommended. The input voltage of the converter is scaled through a voltage divider in order to make it suitable for the AD-Converter. In order to adjust the duty cycle by the digital controller so that the average input current of the converter can follow the reference variable, a STM32F303 evaluation board from STMicroelectronics is used. It is a 32-bit microcontroller clocked with an internal clock frequency of 72 MHz. The detection of the input current and the input voltage of the buck-boost converter as well as the power curve to be controlled are taken over by the internal 12-bit ADC. These analog to digital converted values are then received by the digital control algorithm and creates the necessary PWM signal for

the control of the energy converter switches. Figure 3.41 shows the evaluation board which has to be used.

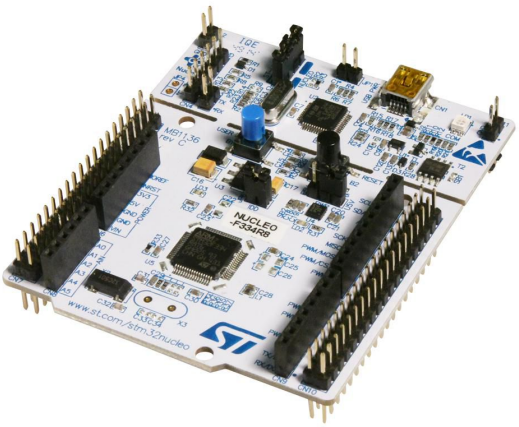

Figure 3.41: Evaluation board to be used for the real hardware setup

4 Experimental Simulation Evaluation of the Energy Storage System

This evaluation is intended to serve as a template for the further real hardware-based system. In this chapter, a verification process is carried out with the model-based hardware implemented design in Matlab Simulink and Plecs Blockset. By starting from the problem definition and the conception of a suitable system structure up to the system design, the technical verification and evaluation can now take place.

4.1 Verification of the Converter System under DC/DC Operation

In this verification, the designed PI-Controller is analyzed under continuous time properties. The measurement simulation setup is build up by the synchronous buck-boost converter together with its sensing stage. For analyzing the closed-loop control structure under DC/DC operation, where three operating points are respectively considered (OP_1, OP_5 and OP_{10}). Those three operating points are the same as in the continuous controller design part in Subsection 3.4.7. The investigation procedure is conducted that the system is stabilized in its steady state value (respected operating point). Afterwards at a specific timestamp an input current step $i_{step}(t)$ is provided and the step response is recorded. Subsequently, the time-based requirements are evaluated on the basis of the step response.

4.1.1 Verfification with Continuous Time Controller

In Figure 4.1, 4.2 and 4.3 the step response results of the closed-loop synchronous buck-boost converter with a unity load step is presented. Let $i_{step}(t)$ the unity input current step be, while the blue signal line represents the input converter current of the analog time model. The red signal behaves according to the obtained control transfer function model $G_{in,d}(s)$.

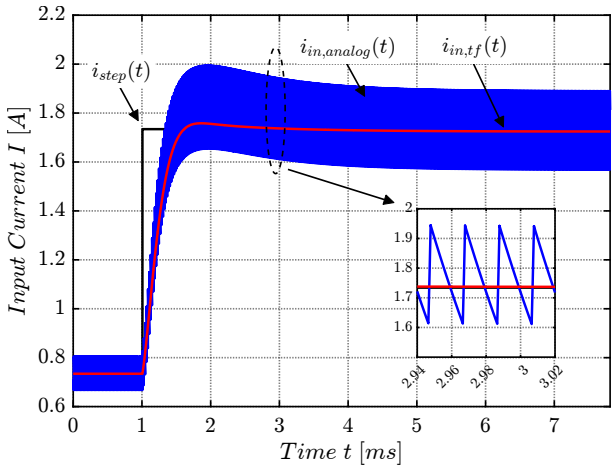

Figure 4.1: Step response of closed-loop system with a load step out of operating point one (OP_1). Operating point is defined at: $I_{in} = 0.73$ A, $D = 0.0674$, $R = 7.53\ \Omega$

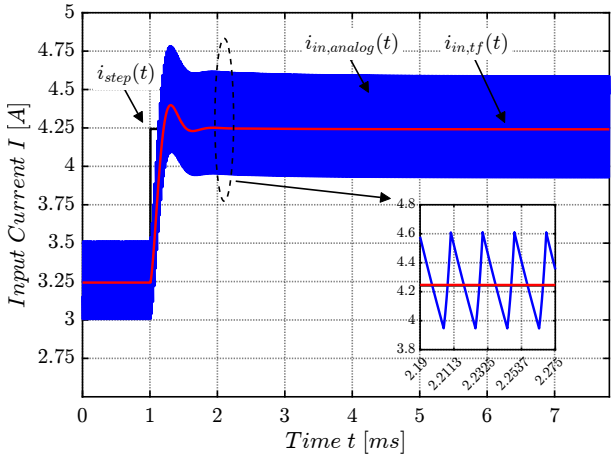

Figure 4.2: Step response of closed-loop system with a load step out of operating point five (OP_5). Operating is defined at: $I_{in} = 3.24$ A, $D = 0.2274$, $R = 21.25\ \Omega$

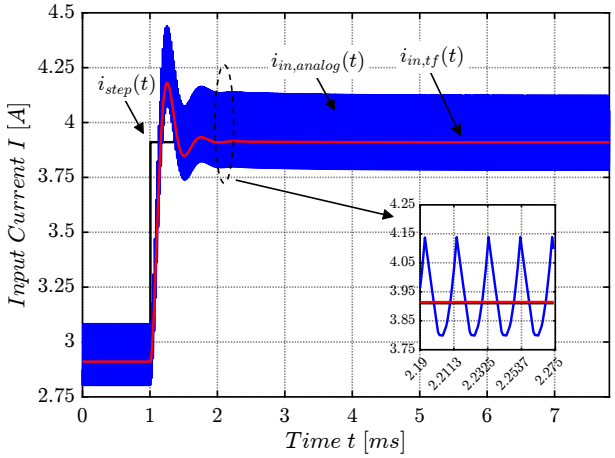

Figure 4.3: Step response of closed-loop system with a load step out of operating point ten (OP_{10}). Operating point is defined at: $I_{in} = 2.91$ A, $D = 0.5928$, $R = 162.93\ \Omega$

The investigation of the performance parameter are shown in Table 4.1.

It is clearly stated that the two models differ sligthly from each other. This fact is related to the modelling and linearization action. A controlled transfer function model of a system does not represent switching moments, so only the average values are available.

Nevertheless, it can be shown that all three selected operating points meet the specification of the time requirements of the control system.

Table 4.1: Performance parameter verification of the continuous closed-loop synchronous Buck-boost converter

Continuous time PI-Controller: $K_P = 16.86e-3$ and $K_I = 12.79$			
Operating Point	Model	Settling Time $[\mathrm{ms}]$	Peak Over Shoot $[\%]$
OP_1	Analaog Circuit	≈ 1.2	3.53
	Control Transfer Function	1.05	2.38
OP_5	Analaog Circuit	≈ 0.6	14.34
	Control Transfer Function	0.49	15.5
OP_{10}	Analaog Circuit	≈ 0.85	30
	Control Transfer Function	0.79	27

It can be shown that the analog circuit model behaves similarly to the control transfer function model. Based on the verification of the continuous control loop, the emulation process from analog controller to digital controller is made. For more information about the analog controller emulation Reference [38] is recommended.

4.2 Verification of the Charging Process under Variable Quantity Conditions

The verification of the charging process under variable quantity conditions simulates the peak power condition under a VLF AC-withstand test situation. The parameterization of the controller parameter are found via the root-locus design technique. In this verification, a comparison is made between the continuous-time control process and the discrete time control process.

4.2.1 Verification with Continuous Time Controller

The implementation of the continuous control loop for the energy storage system is made in the Plecs environment with the control library. Instead of using analogue filters, the internal control filters are used, as for example the mean average filter. Besides this, the model is built up with all its parasitic components. The evaluation of the inductor current, the input converter current and the duty cycle are shown in the following Figure 4.4, 4.5 and 4.6. A direct comparison between the continuous time-controlled signal and the analytically obtained results shall shown that through a proper design procedure similar results can be achieved.

In Figure 4.4 it can be shown that due to the continuous time signal sensing of the input converter current $i_{in}(t)$ an inductor ripple current of $\Delta i_{in} \approx 0.25\mathrm{A}$ appears.

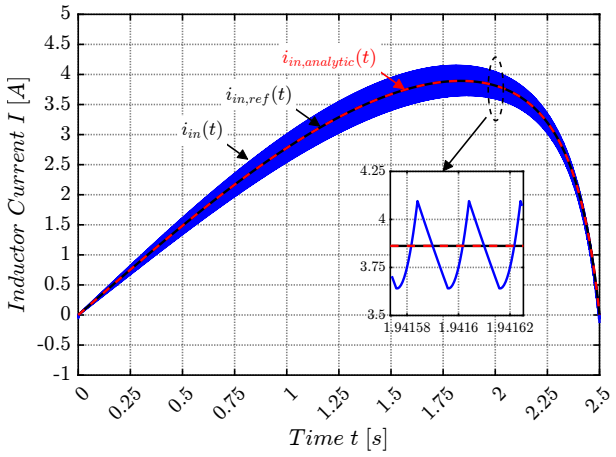

Figure 4.4: Continuous input converter current $i_{in}(t)$ in the continuous control process

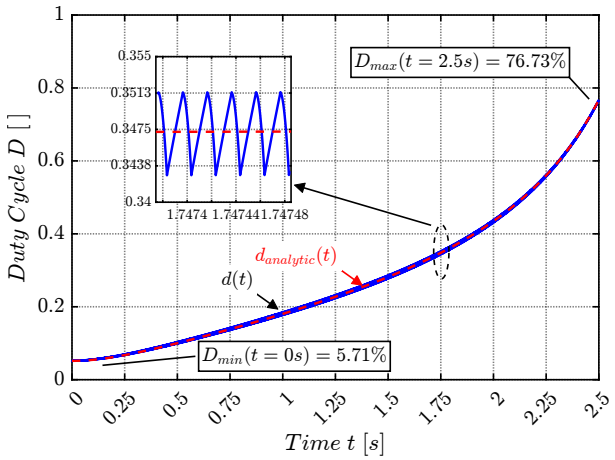

Figure 4.5: Continuous duty cycle $d(t)$ in the continuous control process

In Figure 4.6 a comparison of the analytic inductor current with the continuous inductor current of the energy storage system is shown. The verification shows that over the complete charging process the continuous conduction mode is achieved.

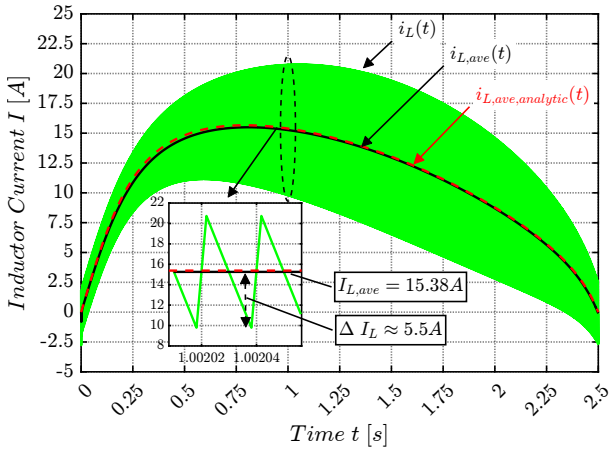

Figure 4.6: Continuous inductor current $i_L(t)$ of the continuous control process is compared against the analytical averaged inductor current

But it has been noted that the ripple inductor current $i_L(t)$ is out of the specification range. In the simulation study, an inductor ripple current of ΔI_L of approximately $5.5\mathrm{A}$ is measured. The averaged mean inductor current $I_{L,ave}$behaves slightly differ compared to the analytical solution.

4.2.2 Verification with Discrete Time Controller

The implementation of the discrete time control process is done by using the C-Script block. The energy storage module is modeled as a capacitor with its ESR. Between the parallel branches of the storage module, no transition resistors are assumed in this investigation. Furthermore, all storage capacitors are always at the same voltage potential and no equalizing currents are expected. With regard to the continuous system, the mean averaged filter block from the continuous time controller is substituted by an analog low pass filter. The implementation of the hardware near simulation composition can be shown up in chapter 3.5. The input voltage $u_{in}(t)$ on the primary side of the converter remains the same as in the analytical preset.

The model setup is specified with a 12-bit ADC with an ADC reference voltage $U_{AD,ref}$ of $3.3\mathrm{V}$. The sampling frequency f_s is defined with $10\mathrm{kHz}$.

In this study the resulting input converter current $i_{in}(t)$ is compared to the reference one $i_{in,ref}(t)$ is shown in Figure 4.7. Additionally, the analytical input current solution $i_{in,analytic}(t)$ of the converter is shown for further comparison. The detailed magnification diagram at timestamp $t \approx 1.94\mathrm{s}$ shows that there is less than two percent difference between the analytical and the digitized input current. This leads to the final result that the control algorithm performs accurately in accordance to the specified control quality requirements from Table 3.20.

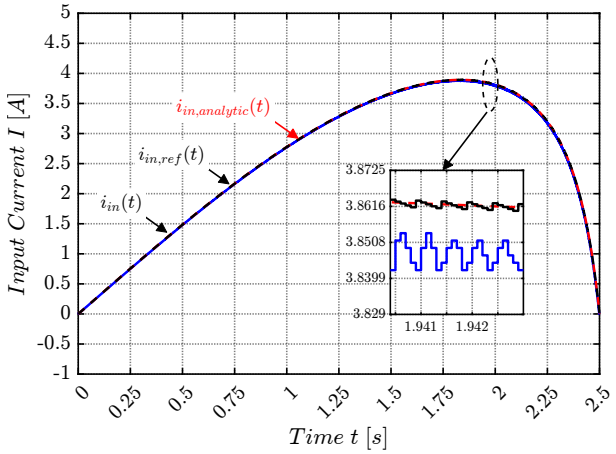

Figure 4.7: Discrete input converter current $i_{in}(t)$ in the digital control process

In Figure 4.8 the obtained control signal $d(t)$ from the PI-Controller and the analytical solution of the control signal $d_{analytic}(t)$ are compared against each other. It can be reflected that the control signal $d(t)$ has a very well agreement to the analytic obtained solution $d_{analytic}(t)$.

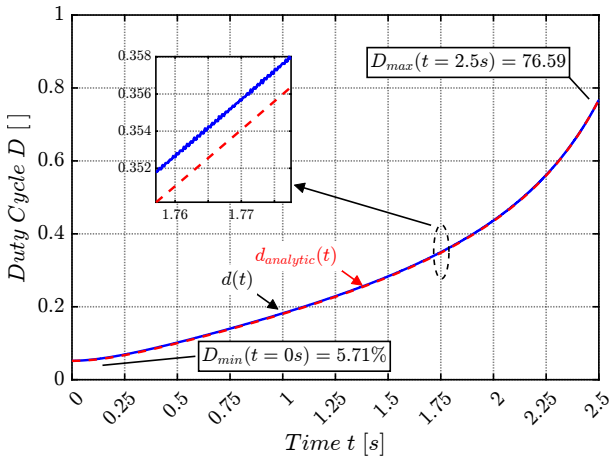

Figure 4.8: Discrete duty cycle $d(t)$ over the charging process

The inductor current in Figure 4.9 allows to investigating whether the converter works in the specified conduction mode. By means of this, the resulting inductor current $i_L(t)$ in the digital controlled scheme reflects that over the complete charging period the continuous conduction mode (CCM) with short phases at the beginning and ending of the forced continuous conduction mode (FCCM) is present. The FCCM mode technique is only valid in synchronous converter topologies. Through the use of this conduction mode, the converter do not operate in the discontinuous mode. In addition, the FCCM itself is only valid under light-load conditions, which are also be found here [39].

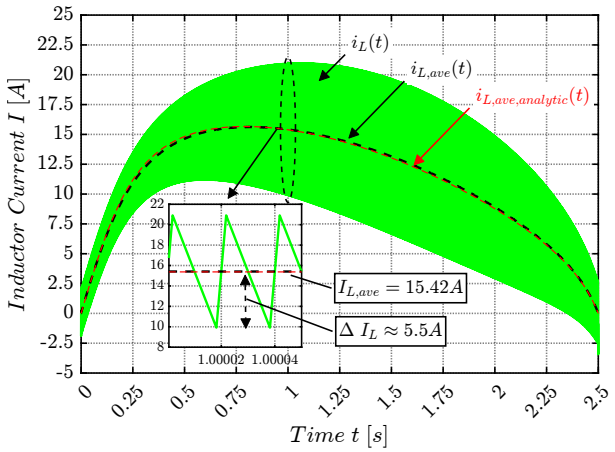

Figure 4.9: Discrete inductor current $i_L(t)$ over the charging process

The advantage of the forced CCM and the conventional CCM are that at a fixed switching frequency can be maintained and the overall inductor ripple current is reduced.

The final storage voltage $u_s(t)$ at the energy storage capacitor unit is illustrated in Figure 4.10. It indicates that the voltage swing from $U_{s,min}$ up to $U_{s,max}$ on the storage system is fully utilized.

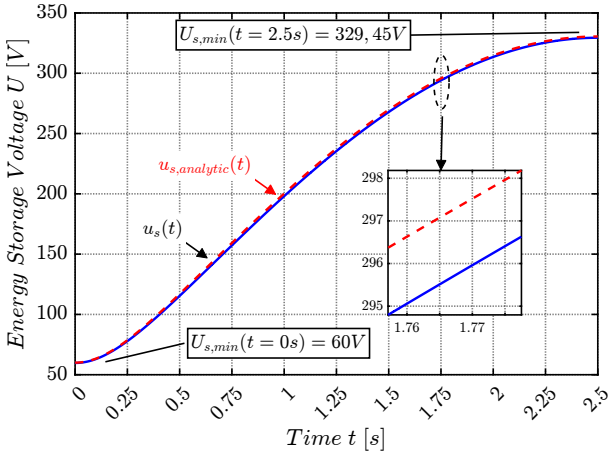

Figure 4.10: Discrete charging voltage $u_s(t)$ at the energy storage device in the digital control case

Due to the specified voltage variability at the energy storage unit, manageable load currents ($i_{in}(t)$, $i_L(t)$) in the converter system could be achieved during the controlled power flow process. In addition, also the requirement for the minimum and maximum storage voltage from Table 1.2 are met.

In Figure 4.11 the total storage charge current $i_s(t)$ and its averaged storage charge current $i_{s,ave}(t)$ in comparison to the analytical charge current solution $i_{s,ave,anyltic}(t)$ is shown.

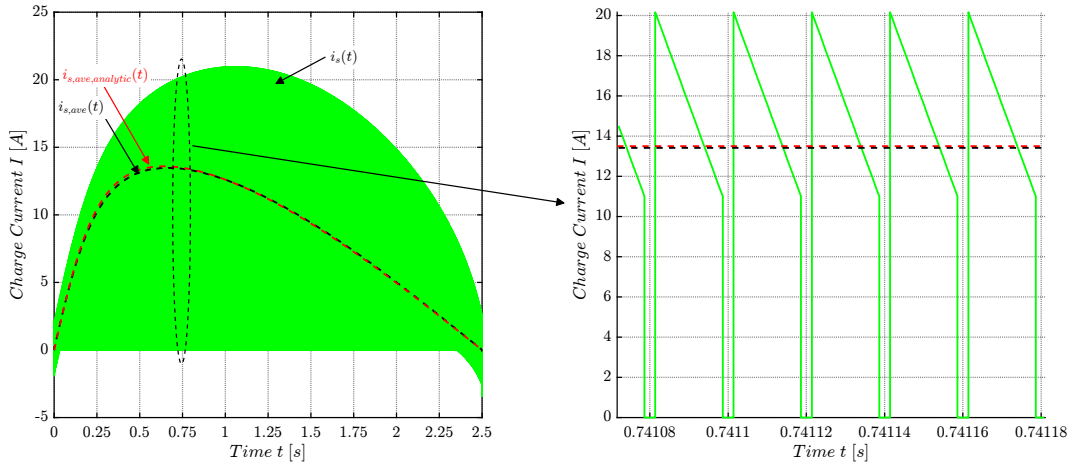

Figure 4.11: Discrete total charging current $i_s(t)$ of the energy storage device in the digital control case

In accordance with the presented Figure 4.11 the maximum charge ripple current is calculated. The ripple current itself plays an important role in terms like equivalent-series-resistor (ESR), overheating, reliability and lifetime and cannot be out of the conversation when verifying such a system. Checking the maximum ripple current provides information as to whether this storage capacitor may be used or not. In order to achieve a longer service life of the storage component, the correct choice of the solution has

to take into account the ripple capacitor current. A comparison with the data sheet maximum ripple current provides then the final suitability of the storage system in the desired application.

Due to this fact the root-mean-square ripple current is calculated by

$$I_{s,Ripple,RMS} = \sqrt{\frac{1}{T_{sw}} \int_{0}^{Tsw} i_s(t)^2 \, dt}. \tag{4.1}$$

Table 4.2 presents the RMS ripple current of the storage system under ideal conditions. The ripple current is responsible for the internal component heat. The rated power dissipation $P_{dis,C}$ in a capacitor can be described by

$$P_{dis,C} = I_{RMS}^2 \cdot R_{ESR}. \tag{4.2}$$

Table 4.2: Maximum ripple current and dissipation loss verification of the aluminium electrolytic storage capacitor modul during the charging phase

Symbol	Meaning	Type Value	Unit
$I_{s,total,Ripple,RMS}$	Total charging ripple current	14.01	$[\mathrm{A}]$
$I_{s,cell1,Ripple,RMS}$	Resulting RMS ripple current single capacitor cell @ maximum current ratings	3.56	$[\mathrm{A}]$
$I_{Ripple,RMS}$	Data-sheet RMS ripple current	37.9	$[\mathrm{A}]$
$P_{dis,C,cell1}$	Disipation loss single cell @ maximum power ratings	0.15	$[\mathrm{W}]$

The given manufacturer's specifications about the ripple current $I_{Ripple,RMS}$ are defined at a certain frequency and temperature. The selected storage capacitor from Kemet have ripple currents $I_{Ripple,RMS}$ of $29.1\mathrm{A}$ (at $100\mathrm{Hz}$, $85°\mathrm{C}$ ambient temperature) and $37.9\mathrm{A}$ (at $10\mathrm{kHz}$, $85°\mathrm{C}$ ambient temperature). It can be seen that no violation of the data-sheet specifications according to the ripple current are caused.

4.2.3 Verification Power Dissipation at the Shunt Resistor

In addition, to the dissipation loss calculation at the energy storage device, the averaged power loss on the shunt resistor is verified too. During the switching phase $D \cdot T_{sw}$ the sense resistor measures the input converter current. The overall averaged power dissipation during the charging process is obtained with

$$P_{dis,shunt,ave} = 0.59 \text{ W}.$$

The occurring peak power dissipation of the shunt resistor at the maximum input converter current is

$$P_{dis,shunt,peak} = 7.8 \text{ W}.$$

The dissipation power of the shunt resistor is below the maximum power loss of 10W which is specified by the manufacturer. The bill of material with its component and its specifications is given in Subsection 3.5.1.

4.2.4 Verification Sensed Input Current to Reference Input Current

In this verification the digitized sensed input current $i_{in}(t)$ is compared with the reference input current $i_{in,ref}(t)$. By means of this, the synchronous sampling strategy which is mentioned in Section 3.5 will be analysed in a more detailed sense.

In Figure 4.12 the input converter current in analog and digital domain are shown. Let $i_{in}(t)$ the sampled discrete input current. The filtered analog input current signal is represented by the $i_{in,filtered,analog}(t)$.

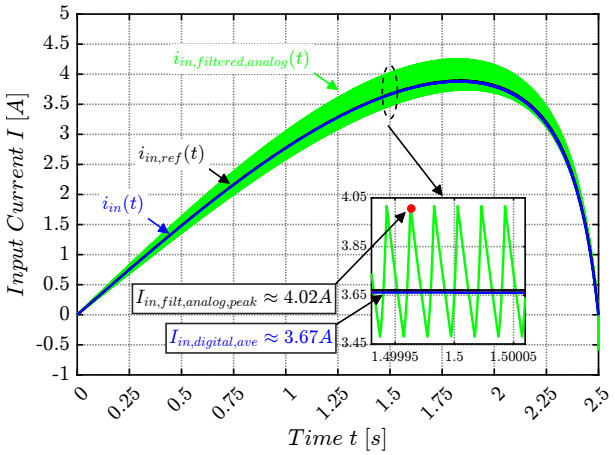

Figure 4.12: Input converter current $i_{in}(t)$ of analog and digital domain over the complete charging process

It is remarkable that if no synchronous sampling would be implemented, the control system must be able to compensate a percentage input current measurement deviation ΔI_{in} of $\approx 10\%$ in worst case conditions. If this does not happen, an unstable control loop would be the result. The measurement deviation is calculated by

$$\Delta I_{in} = \frac{I_{in,filt,analog,peak}}{I_{in,digital,ave}} \cdot 100\%. \tag{4.3}$$

The reason behind this strategy is based on the fact that by including a low-pass filter of lower cut-off frequency, will cause the converter system to slow down tremendously. By attempting to smooth the input current without visible switching cycles will then result in a tremendous slow system dynamic and can lead together with the closed-loop control system to instability problems.

4.3 Summary Experimental Verification

The continuous time controller is verified in the first part of the experimental simulation study under DC/DC converter conditions. In this examination the continuous circuit model is compared against the control transfer function model $G_{in,d}(s)$. The designed controller works in accordance to the specifications in different operating points of the energy recovery phase. The performance time based requirement parameters are reached in all respected operating points. Table 4.1 summarizes the performance measure. A discretization of the continuous closed-loop system was not performed for this verification. The reasons are related to the fact that due to the converters switching moments the switching frequency ($f_{sw} = 50\mathrm{kHz}$) in the Fourier series still shows significant amplitude values. According to Nyquist-Shannon sampling theorem, a sampling frequency of several kHz would be necessary in order to guarantee almost an equivalent control behaviour of the input current. Since a very slow dynamic time-changing behaviour of the energy recovery system is given, an exact replication of the waveform is not of particular necessity.

In the second part of the simulation analysis, the complete charging operation between continuous and discrete-time system has been verified. The main task of this study is to show again the differences between continuous and discrete control behaviour. The main goal of a digital control structure could be achieved by emulating the continuous control system. Step by step, the digital control system has been abstracted from a nearly continuous frequency range to a sampling interval T_s of $0.1\mathrm{ms}$ without obtaining any unstable control behaviour. Subsequently, a comparison could be carried out. A final verification of the charging currents using the ripple current analysis for the storage capacitors has been done. This has provided information about the suitability of the storage concept. The maximum measured capacitor ripple current does not exceed the manufacturer-specific specifications.

5 Summary and Outlook

5.1 Summary

In this thesis a design concept for the elaboration of a proof of concept for the integration of an energy storage system in a VLF generator was presented, analyzed and verified. One of the central components in the overall system is the energy storage unit. The objective was to define a model-based hardware implementation of the developed energy storage system in Matlab Simulink an Plecs Blockset. The application environment, the high discharge energy quantities, the short discharge period and their power curve are particularly important for the selection of the energy storage element. Based on a utility analysis, it became apparent that the aluminium electrolytic capacitor storage variant is the most suitable for storing the discharge energy, not at least because of the simple realization of the storage module, but also because of the high nominal voltage. In addition to this different converter topologies were investigated.

It has been found out that the synchronous buck-boost converter emerged as a suitable circuit topology for controlling the power flow in the discharge phase. This was mainly due to the fact that this variant has a high degree of industrialization and flexibility thanks to the H-Bridge. Subsequently, the selected topologies (aluminium electrolytic capacitor and synchronous buck-boost converter) were adapted to the desired application based on the specified requirements. Through an analytical examination of the energy storage process, important information on the charging current and charging voltage at the input of the energy storage element and at the output of the converter could then be calculated. This analytical information was then merged with the steady state analysis of the converter. The aim was to find relationships to determine the average inductor current as well as the input current of the converter. This theoretical solution was then further intensified and an analytical solution for the control of the H-bridge was also found. These analytic average current and voltage signals were then used to dimension the storage inductor and MOSFET. With support of a developed AC model of the converter, by using the state-space-averaging technique, it was possible to investigate the dynamic behaviour of the energy storage system in a large number of operating points during the energy recovery process. Using control engineering analysis methods, important findings on the dynamic behaviour were extracted and then taken into account for the controller design. A PI controller and the control of the input current at the energy storage system turned out to be advantageous.

By applying the emulation process, the analog controller has been converted into a dig-

ital controller and was then inserted into the model-based hardware implementation. It became evident that the digital control loop in the simulation with a target sampling frequency of $10\mathrm{kHz}$ and an ADC resolution of 12-bit works sufficiently accurately for the energy storage system. The current and voltage results showed that the required spectrum of requirements were largely fulfilled. However, the simulation result for the inductor current showed a clear deviation from the defined ripple inductor current. Approaches for the reduction of the increased ripple inductor current were presented. These approaches could then be tested by further experiments. The loss mechanism at the power semiconductors were analysed by using the double-pulse-switching test. The switching and conduction losses were modelled and simulated by a circuit simulation with the software LTSpice. Due to the ongoing pulse operation during the energy transfer from the primary side to the secondary storage side of the converter, a pulse strength analysis was performed on the storage capacitor. The alternating component of the charging current, also referred to as ripple current, was examined. Concerning the ripple current, no deviations from the data-sheet specifications were found. This result confirms the suitability of the energy storage device in the current application.

5.2 Outlook

This thesis dealt with the modeling of an energy storage system on simulation basis in order to enable a first statement about the feasibility of the storage system in a VLF generator application. In the course of this thesis, a design process for the selection of suitable system modules was developed. A simulation study of the model-based hardware implemented energy storage system with a digital control strategy was then used to clarify initial fundamental questions. Nevertheless, the results can now be used to formulate further interesting starting points for future investigations:

- The storage inductor was designed using the Kg-method. Subsequent control calculations have shown that the inductor design method is valid. Based on the dimensioned inductor, an initial hardware sample can now be created. By means of a RLC measuring device, the series and parallel capacitor, resistor values can be determined. An additional impedance analysation with the vector network analyser Bode 100 can also be done. These quantities can then be taken into account in further simulation experiments.
- No loss calculation was performed for the coil. Only the skin effect was taken into account when selecting the conductor for the inductance. Ideal winding arrangement were assumed, in a way that no proximity effects would occur. In order to make a theoretical statement about the loss behaviour of the coil, one could calculate the DC losses, the AC losses and the core losses. This offers another research point, in which the inclusion of these sources of loss and the study of their impact on the system can be investigated.
- According to Subsection 3.4.5, for the operation of the converter in the energy recovery phase, the input current was measured and controlled by a PI-Controller. Two half-bridge drivers were used to control the H-Bridge. The input current was measured by the shunt resistor on the low side. Based on this sensing setup, the question arises to what extent this sense resistor influences the control of the MOSFET.
- Ideal capacities were assumed for the evaluation of the energy storage module and its behaviour. Each storage capacitor cell therefore always has the same cell voltage and no equalizing currents are flowing. The fact that voltage drops occur due to additional contact resistances between the modules yields to a change in the capacitors charging voltage from cell branch to cell branch. Additionally a low-pass filter with each parallel capacitor branch is built up. It could be therefore investigated how the energy storage system behaves with different capacity values and contact resistances with regard to current and voltage.
- Optimizations with regard to the overall system were not taken into account. The primary objective was to check the feasibility. Hereby, no cost and volume points were considered for the current model-based hardware implemented energy storage system. The question therefore arises to what extent the energy storage units

can be reduced in size and weight for this application. The objective should be to define an energy storage variant with high capacity and voltage ratings.

- During the verification, no detailed modelling for efficiency prediction was performed on the model-based hardware implemented energy storage system. This has to do with the fact that the Plecs environment does not allow to implement third-party models. Further research could therefore be done by building up a scaled version of the energy storage system to verify the charging process. In this way additional thermal aspects can be considered.
- Based on the feasibility study through the verification of the charging phase, all required specifications could be implemented. In addition, an analysis of the power losses on the individual components was carried out. In the further development of the energy storage system, the next step could focus on system integration. The question here is at which interfaces the stored energy is ultimately released again. Topics such as efficiency, use and their integration are to be examined.

Bibliography

[1] M. Kamran, "(chapter 3)power electronics for renewable energy systems," in Renewable Energy Conversion Systems, M. Kamran and M. R. Fazal, Eds. Academic Press, 2021, pp. 53–108. [Online]. Available: https://www.sciencedirect.com/science/article/pii/B9780128235386000014

[2] S. Koohi-Fayegh and M. Rosen, "A review of energy storage types, applications and recent developments," Journal of Energy Storage, vol. 27, p. 101047, 2020. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S2352152X19306012

[3] P. Spichartz, P. Dost, and C. Sourkounis, "Recuperation strategies for electric vehicles," in 2014 Ninth International Conference on Ecological Vehicles and Renewable Energies (EVER), 2014, pp. 1–7.

[4] J. J. Mwambeleko and T. Kulworawanichpong, "Supercapacitor and accelerating contact lines hybrid tram system," Journal of Energy Storage, vol. 44, p. 103277, 2021. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S2352152X21009713

[5] N. Rosle, N. A. Muhamad, M. N. K. H. Rohani, and M. K. M. Jamil, "Partial discharges classification methods in xlpe cable: A review," IEEE Access, vol. 9, pp. 133 258–133 273, 2021.

[6] S. Filiz and U. Yunus, "A comparative study: voltage multipliers for rf energy harvesting system," Communications Faculty of Sciences University of Ankara Series A2-A3 Physical Sciences and Engineering, vol. 61, no. 1, pp. 12–23, 2019.

[7] D. Suksawat, T. Hengcharoensuk, T. Nupinit, K. Chusang, T. Ravangvong, and N. Pattanadech, "Investigation of very low frequency dissipation factor of the contaminated underground cable joints," in 2020 8th International Conference on Condition Monitoring and Diagnosis (CMD), 2020, pp. 342–345.

[8] P. Naveen, M. R. Rao, N. Krishna, and A. Ambekar, "Kinetic energy recovery system," 2014.

[9] K. Schneider, "Liebherr pactronic–hybrid power booster," Wie [9.54], pp. 163–171, 2011.

[10] D. A. Hewitt, J. E. Green, J. N. Davidson, M. P. Foster, and D. A. Stone, "Observation of electrolytic capacitor ageing behaviour for the purpose of prognostics," in

IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society, 2016, pp. 2195–2200.

[11] S. A. Gorji, H. G. Sahebi, M. Ektesabi, and A. B. Rad, "Topologies and control schemes of bidirectional dc–dc power converters: An overview," IEEE Access, vol. 7, pp. 117 997–118 019, 2019.

[12] R. W. Erickson and D. Maksimovic, Fundamentals of Power Electronics, 2nd ed. Springer, 2001.

[13] M. Sterner and I. Stadler, Energiespeicher - Bedarf, Technologien, Integration. Springer Berlin Heidelberg, 2014. [Online]. Available: https://books.google.at/books?id=MFajBAAAQBAJ

[14] J. Artal-Sevil, R. Bandrés, and G. Fernández, "Ulises: Autonomous mobile robot using ultracapacitors-storage energy system," Renewable Energy and Power Quality Journal, pp. 1105–1110, 05 2011.

[15] R. T. Yadlapalli, R. R. Alla, R. Kandipati, and A. Kotapati, "Super capacitors for energy storage: Progress, applications and challenges," Journal of Energy Storage, vol. 49, p. 104194, 2022. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S2352152X22002262

[16] M. Rosu, U. Deshpande, and J. M. Miller, "Carboncarbon ultracapacitor equivalent circuit model, parameter extraction, and application."

[17] L. Zhang, X. Hu, Z. Wang, F. Sun, and D. G. Dorrell, "A review of supercapacitor modeling, estimation, and applications: A control/management perspective," Renewable and Sustainable Energy Reviews, vol. 81, pp. 1868–1878, 2018. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S1364032117309292

[18] A. Burke, "Ultracapacitors: why, how, and where is the technology," Journal of Power Sources, vol. 91, no. 1, pp. 37–50, 2000. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0378775300004857

[19] M. E. Şahin, F. Blaabjerg, and A. Sangwongwanich, "A comprehensive review on supercapacitor applications and developments," Energies, vol. 15, no. 3, 2022. [Online]. Available: https://www.mdpi.com/1996-1073/15/3/674

[20] V. Lorentz, "Bidirectional dc voltage conversion for low power applications," Ph.D. dissertation, 01 2009.

[21] K. Tytelmaier, O. Husev, O. Veligorskyi, and R. Yershov, "A review of non-isolated bidirectional dc-dc converters for energy storage systems," in 2016 II International Young Scientists Forum on Applied Physics and Engineering (YSF), 2016, pp. 22–28.

[22] D. Ravi, S. S. Letha, P. Samuel, and B. M. Reddy, "An overview of various dc-dc converter techniques used for fuel cell based applications," in 2018 International

Conference on Power Energy, Environment and Intelligent Control (PEEIC), 2018, pp. 16–21.

[23] H.-S. Lee and J.-J. Yun, "High-efficiency bidirectional buck–boost converter for photovoltaic and energy storage systems in a smart grid," IEEE Transactions on Power Electronics, vol. 34, no. 5, pp. 4316–4328, 2019.

[24] S. Cuk, "A new zero-ripple switching dc-to-dc converter and integrated magnetics," IEEE Transactions on Magnetics, vol. 19, no. 2, pp. 57–75, 1983.

[25] J. Majo, L. Martinez, A. Poveda, L. de Vicuna, F. Guinjoan, A. Sanchez, M. Valentin, and J. Marpinard, "Large-signal feedback control of a bidirectional coupled-inductor cuk converter," IEEE Transactions on Industrial Electronics, vol. 39, no. 5, pp. 429–436, 1992.

[26] R. D. Middlebrook, S. Cuk, and W. Behen, "A new battery charger/discharger converter," 1978 IEEE Power Electronics Specialists Conference, pp. 251–255, 1978.

[27] J. Meher and A. Gosh, "Comparative study of dc/dc bidirectional sepic converter with different controllers," in 2018 IEEE 8th Power India International Conference (PIICON), 2018, p. 1 to 6.

[28] A. Cantillo, A. DeNardo, N. Femia, F. Forrisi, A. Russo, and W. Zamboni, "Sepic design- part ii: Capacitive damping," 12 2009, pp. 1724 – 1729.

[29] J.-J. Chen, P.-N. Shen, and Y.-S. Hwang, "A high-efficiency positive buck–boost converter with mode-select circuit and feed-forward techniques," IEEE Transactions on Power Electronics, vol. 28, no. 9, pp. 4240–4247, 2013.

[30] V. Vorperian, "Simplified analysis of pwm converters using model of pwm switch. ii. discontinuous conduction mode," IEEE Transactions on Aerospace and Electronic Systems, vol. 26, pp. 497–505, 1990.

[31] Ferrites and Accessories, Std., Jul. 2022. [Online]. Available: https://www.tdk-electronics.tdk.com/en/ferrites

[32] H. Gui, Z. Zhang, R. Ren, R. Chen, J. Niu, L. M. Tolbert, F. Wang, B. J. Blalock, D. J. Costinett, and B. B. Choi, "Sic mosfet versus si super junction mosfet-switching loss comparison in different switching cell configurations," in 2018 IEEE Energy Conversion Congress and Exposition (ECCE), 2018, pp. 6146–6151.

[33] How to Select the Right CoolMOS and its Power Handling Capability, V1.2 ed., Jan. 2002, application Note. [Online]. Available: https://www.infineon.com/dgdl/Infineon-ApplicationNote_MOSFET_CoolMOS_How_to_select_the_right_CoolMOS-AN-v01_00-EN.pdf?fileId=db3a304412b407950112b40acf580693

[34] B. Bequette, Process control: modeling, design, and simulation, 1st ed. Upper Saddle River, NJ, USA: Prentice Hall Press, 2002. [Online]. Available: http://portal.acm.org/citation.cfm?id=1405709&dl=GUIDE&coll=GUIDE

[35] T. Graz, Regelungstechnik 1. Institut für Regelungstechnik und Automatisierungstechnik, 2020. [Online]. Available: https://www.tugraz.at/fileadmin/user_upload/Institute/IRT/Aufgabensammlung/Regelungstechnik_I/Regelungstechnik_1.pdf

[36] A. H. u. K. S. F. Gausch, Digitale Regelkreise. Institut für Regelungstechnik / Technische Universität Graz, 1991. [Online]. Available: https://www.tugraz.at/fileadmin/user_upload/Institute/IRT/Buecher_Software/DigiReg.pdf

[37] Plexim, Introduction to the C-Script Block, tutorial version 1.0 ed., first release. [Online]. Available: https://www.plexim.com/sites/default/files/tutorials/cscript_controller.pdf

[38] D. L.Plett, Emulation of Analog Controllers, online ed., Aug. 2022. [Online]. Available: http://mocha-java.uccs.edu/ECE5540/ECE5540-CH02.pdf

[39] P. Guan, “Chapter 57-cascadable 7a point-of-load monolithic buck converter,” in Analog Circuit Design, B. Dobkin and J. Hamburger, Eds. Oxford: Newnes, 2015, p. 123 124. [Online]. Available: https://www.sciencedirect.com/science/article/pii/B9780128000014000570

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